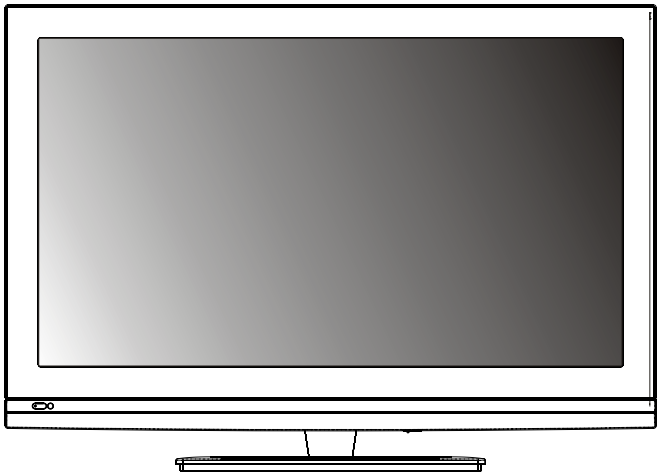
SERVICE MANUAL

8M79B CHASSIS



Design and specifications are subject to change without prior notice.
(Only Referrence)

SIZE:A5

Description:	SERVICE MANUAL 8M79B	
MODEL.	Brand Name:	SKYWORTH
JOB NO.		
Engineering Dept:		
Artwork By:	Date:	2012-02-04
Checked By:	Date:	
Approved By:	Date:	

Content

Technical Specification

1.Application Area:

This product standard is used for LCD 8M79B chassis.

2.Specification:

All the standard are measured under following conditions without other specification.

2.1 Ambient Temperature:20+/-5℃

2.2 Relative Humidity:65+/-10%

2.3 Power Supply Voltage: Standard Input Voltage(100V~240Vac 50/60Hz)

2.4 Adjust after 20 minutes warm-up.

3.Test and check method:

3.1 Capability:According to nation test standard

3.2 Safety:_____ standard

EMC:_____ standard

4. Safety and Regulation

No	Item	Min	Typ	Max	Unit	Remark
1.	Force Stability – Incline Plane Tip Test		10		deg	
2.	Force Stability – Level Tip Test		100		N	
3.	Isolation Gap, AC-AC/ AC-DC	3			mm	
4.	Isolation Gap	6			mm	
5.	Power Consumption, Max		65		W	For 32LED
			120		W	For 42LED
					W	
6.	Power Consumption, Stand by			1	W	
7.	Dielectric Voltage	3			kV	
8.	Isolation Resistance	4			MΩ	
9.	Leakage Current		5		mApp	
10.	Power Cord Captivity		40		N	
11.	Flammability – Back Cover		PASS			
12.	Sharp Edge		PASS			
13.	UL Compliance		NO			
14.	FCC Compliance		NO			
15.	CDRH Radiation Compliance		NO			
16.	CSA Compliance		NO			
17.	CEB Compliance		NO			
18.	CE Compliance					Base on different order
19.	CB Compliance		YES			

5. Video

No	Item	Min	Typ	Max	Unit	Remark
1.	Linearity Distortion, Vertical		1		%	
2.	Linearity Distortion, Horizontal		1		%	
3.	Trapezoidal Distortion, Vertical		1		%	
4.	Trapezoidal Distortion, Horizontal		1		%	
5.	Over Scan, Vertical	93	95	97	%	
6.	Over Scan, Horizontal	93	95	97	%	
7.	Brightness, Maximum		400		cd/m^2	FOR 32LED
			450		cd/m^2	FOR 42LED
					cd/m^2	
8.	Video Noise Limited Sensitivity(@S/N=30db) VHF			51	dBUV	
9.	Video Noise Limited Sensitivity(@S/N=30db) UHF			54	dBUV	

10.	Selectivity -1.5M	35			dB	
11.	Selectivity +8M	40			dB	
12.	Tuning Range	-0.7			MHz	
13.	Resolution Horizontal		1366		Lines	1920 For 42LED
14.	Resolution Vertical		768		Lines	1080 For 42LED

6. Chroma

No	Item	Min	Typ	Max	Unit	Remark
1.	White Balance, X axis		280			
2.	White Balance, Y axis		290			
3.	White Balance, Color Temperature	6500	9800	12500	kdeg	12500(266, 276) 9800(280, 290) 6500(313, 329)
4.	Color Sensitivity		30		dB	
5.	Color Burst Lock-in Range	+/-300			Hz	
6.	Color Killer Sensitivity		30		dBuv	

7. Audio

No	Item	Min	Typ	Max	Unit	Remark
1.	Audio Noise Limited Sensitivity, VHF-L		25		dBuv	
2.	Audio Noise Limited Sensitivity, VHF-H		25		dBuv	
3.	Audio Noise Limited Sensitivity, UHF		28		dBuv	
4.	Buzz (S/N Ratio)		40		dB	
5.	Distortion		3		%	
6.	Audio Output, L/R,at 10% THD		8		W	
7.	Audio Output, Center		8		W	
8.	Stereo Separation		21		dB	
9.	Speaker Impedance		8		ohm	
10.	Speaker Power Rating		10	15	W	

8. Power

No	Item	Min	Typ	Max	Unit	Remark
1.	DC Voltage, Audio		24		V	
2.	DC Voltage, Tuner(5)		5		V	

9. External Interface

No	Item	Min	Typ	Max	Unit	Remark
1.	Video Input Level		1		Vpp	75 OHM
2.	Video Input Frequency Response	4.5			MHz	
3.	Video Input S/N		40		dB	
4.	Audio Input Level		0.5		Vrms	
5.	Audio Input Frequency Response			15	kHz	
6.	Audio Input S/N		40		dB	
7.	Audio Input Distortion		3		%	
8.	Audio Input Dynamic Range			2	V	
9.	Video Output Level		1		Vpp	
10.	Video Output Frequency Response		4.2		MHz	
11.	Video Output S/N		50		dB	
12.	Audio Output Level		0.5		Vrms	
13.	Audio Output Frequency Response	80		12000	Hz	
14.	Audio Output S/N		40		dB	
15.	Audio Output Distortion		6		%	

16.	Video Input Level, R/G/B		0.7		Vpp	
17.	Video Input Level, Component(Y, P_B, P_R)		0.7		Vpp	75 ohm
18.	RGB Input Resolution, Vertical		768		pixel	1080 For 42LED
19.	RGB Input Resolution, Horizontal		1366		pixel	1920 For 42LED
20.	RGB Input Horizontal Frequency		68		kHz	
21.	RGB Input Frame Rate		60		Hz	

10. The others

No	Item	Min	Typ	Max	Unit	Remark
1.	Search Sensitivity		40		dBuv	
2.	Clock, real time gain or loss (sec per day)		NO		sec	
3.	Soft Ware Functionality Test		YES			
4.	REMOCON Working Sensitivity, Straight		8		m	
5.	REMOCON Working Sensitivity, T/B/L/R		6		m	
6.	Closed Caption Sensitivity		46		dBuv	
7.	Teletext Sensitivity		46		dBm	
8.	Resonance of unit (Sweep freq : 50 ~ 1000)		NO			

11. Customer Menu Setup (as shipped condition)

No	Item	Specification	Remark
1.	PSM	Standard	
2.	SSM	Standard	
3.	Volume	20	
4.	Mute	Off	
5.	Input Mode	RF	
6.	Customer Menu Language	English	Base on different order
7.	AVL	Off	
8.	Sleep Timer	Off	
9.	Auto Sleep	Off	
10.	Blue Back	No	
11.	Surround	Off	
12.	Caption	Off	
13.	Noise Reducer	Middle	"Low" in some status

12. Reliability

No	Item	Min	Typ	Max	Unit	Remark
1.	ESD		4		kV	IEC-1000-4-2
2.	EFT/Burst				kV	IEC-1000-4-4
3.	Surge Immunity				kV	IEC-1000-4--5
4.	Voltage Dip Test, 10ms				%	IEC-1000-4-11
5.	Voltage Dip Test, 100ms				%	IEC-1000-4—11
6.	Operation Temperature				deg	
7.	Operation Humidity				%	
8.	Storage Temperature				deg	
9.	MTBF (Confidence Level : 90 %)				hour	

DTV-PRODUCTOINS SPECIFICATION

Model #	**42"～55"**
Country(West Eu./East Eu./Russia/AP/US/S.A./Japan/…)	Brazil & Argentina
Brand	Skyworth/ODM
Category (Monitor/TV/Combo/Portable TV…)	TV
Panel technology (LCD / PDP)	LED
Market Position (High/Mid/Access,,,)	Class
Cabinet Design (Example: 01,23 series)	E72
Product Nb	-
Chassis solution	MSD309 + ISDB-T Demod
Chassis name	8M79B
Chassis PCB Standard	Skyworth RGB New Standard
Predecessor (replace)	-
MP date requested (ETD)	2011.8
MP date confirmed by supplier (ETD/ETA)	-
Status(Pre./Finish)	-
Regional requirement	
Homologation (Gostandard/CE/MPTT/CB/…)	CB
RoHS	Yes
Power supply(100-240V AC +/-10%/...)	100-240V AC (-20%,+10%)
Power consumption working / Annual	-
Power consumption standby	<1W
Power plug(VDE/UL/BS/…)	UCIEE/2pins
Picture display	
Screen size : diagonale (inch)	42", 47",55"
Aspect ratio (16/9 // 4/3 // 15/9)	16:9
1st panel supplier : panel suppliers	LG
1st panel supplier : panel reference	
Panel Display Type(MVA/PVA/IPS/…)	TFT LCD
1st panel supplier : resolution	42/47/55:1920x1080
Dynamic contrast ratio	**>10000：1**
Video signal process	
Comb Filter (2D/3D)	3D
Noise Reduction (adaptative/3D/…)	3D
Picture improvement (LTI/CTI,BLE,WLE,...)	LTI/CTI
Color process (Gama correction/Skin correction /...)	Follow main IC
Colour preset (Cool/Normal/Warm/Personal)	Neutral, Cool, Warm and Personal in PC mode
Picture control (Bright/Con./Sharpness/Color/Tint/…)	Yes
Picture presets : Standard / Bright / Soft / User	Normal / Soft / Personal / Bright

Technical Specification

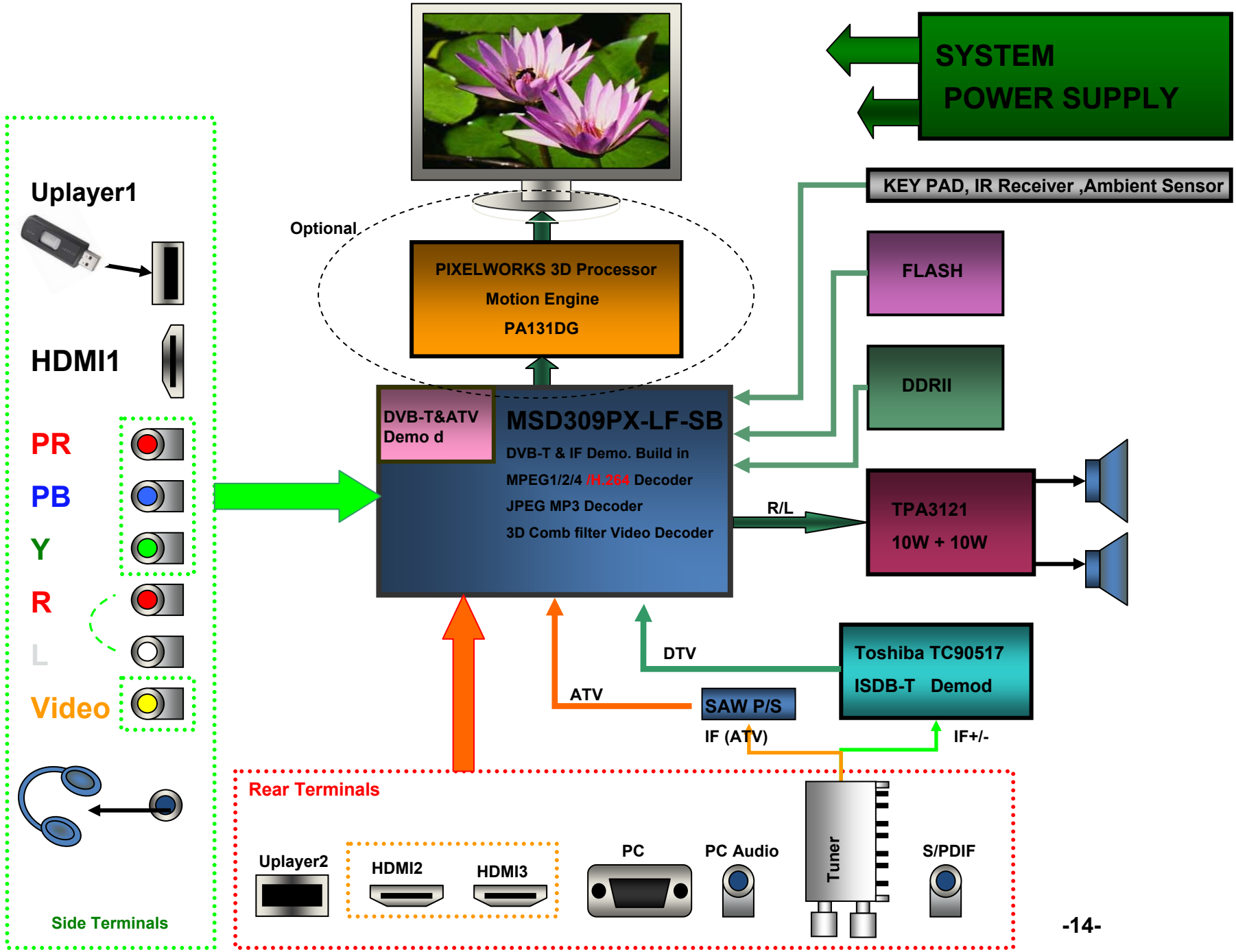
Picture freeze	Yes
Multi picture : PIP (AV)/POP（AV）	No
Dynamic Backlight Control	**No**
LED Backlight	Yes
Deinterlacer (No/linerar/motion adaptive/motion compensative)	3D motion adaptive
Film mode / reverse 3:2/2:2 pull down	Yes / Yes
Full HD support (1080P)	Yes
Single scan / Dual scan (120HZ)	Single scan
Zoom type : 4/3 format	Yes
Zoom type : 14/9 Zoom	**Yes**
Zoom type : 16/9 Zoom	16/9 ZOOM 1
Zoom type : 16/9 Zoom up/down	16/9 ZOOM 2
Zoom type : Cinerama	Yes
Zoom type : 16/9 Format	Yes
Zoom type : Auto (by SCART Pin8 and WSS)	Yes
Picture Auto adjustment (PC mode)	Yes
3D Panel Type(PR / SG)	PR
3D Mode	Left/Right, Up/Down, Frame Sequence
3D To 2D (Y/N)	Yes
2D To 3D (Y/N)	Yes
Left / Right Swap (For PR Panel)	Yes
Sound	
Sound type (Mono/AV stereo/Stereo)	stereo
Music Power (Watt)/RMS Power (Watt)	2 x 8W
Tone control (Bass&Treble / Graphic Equalizer)	Bass&Treble
Special sound effect (AVL / WIDE / Pseudo /…)	AVL
Suround system (Dolby / VD / SRS / BBE / …)	Built-in Surround
Sound control (Volume , Balance , Mute)	Volume, Balance, Mute
Sound presets (User/Speech/News/Standard)	Standard / Music / Film / News / Personal
Headphone volume control (Separated / linked)	**Yes(Linked)**
Sound quality (High / Mid / Low)	Mid
Reception and Decoding capability	
RF range（ATV）	**54MHz～864MHz**
RF range（DTV）	**VHF 177-213 MHZ, UHF 473-803 MHZ**
Color System (PAL/SECAM/NTSC/PAL M,N)	PAL M,PAL N,NTSC M
Audio Standard (B/G/H/D/K/K'/I/L/L')	M,N
Stereo audio system (Nicam,MTS,A2,….)	BTSC,SAP
Video standard NTSC 3.58 / 4.43 (AV)/PAL 60	NTSC 3.58/4.43 , PAL
DTV SD support (DVB-T/S/C , ATSC , QAM , …)	ISDB-T
DTV HD Support	MPEG2,MPEG4,H.264
MHEG5	No
HD capability with YPbPr	Yes (720p; 1080i; 1080p@24/50/60Hz; 480i/p; 576i/p)
PC capability (up to maximum format)	Up to 1280X1024 60Hz
HDMI capability （AV/PC Format)	Up to 1080P 24/50/60HZ
Compatible video format if DVD/USB: DviX/VCD/SVCD/JPEG/AVI/MPEG2/WMV- HD/SD	JPEG/MPEG2/MPEG4/H.264/DivX (depending on license)

Compatible audio format if DVD/USB: MP3/WMA/AAC/MPEG1/…	MP3/WMA(depending on license)
Playable Discs (CD/CD-R(RW)/CD-ROM/DVD+R/+RW/-R/-RW)	No
Card reader format compatibility	No
Macrovision	Yes
PVR	Yes（FOR USB）
Network	No
User convenience	
OSD Language*	English/Spanish/Portuguese/French
OSD Positioning	No
OSD Transparency Adjust	No
OSD Timeout Adjust	No
Customer Brand name(LOGO)	Yes
IB languages	English
ATV Program Numbers (example: 99+3AV input)	99+7AV
DTV Program Numbers	370
Program edit (naming , sorting , skip , swap ….)	Skip / Delete
Auto Naming/Auto Sorting	No
TV Guide(DTV EPG)	EPG(next Seven-day)
Favorite program	Yes
Number of buttons on cabinet (Power; Vol+/-; Pr+/-, Menu)	Vol+/-; CH+/-, Menu ,Source,Standby(optional)
Main switch button (yes/No)	Yes
CCD（Closed Caption)/V-CHIP	Yes/No
Text Standard: (Top, FLOF,,,)	No
Teletext Level: 2.5 / 1.5	-
Pages for teletext	-
Teletext character sets ****	-
DVB-T teletext	-
Real clock	From DTV
Sleep timer	10-240 Min.
Timer	Turn On / Off, Program Switch
Parent Control -Source and Channel lock (Input code for certain channel)	Yes
Parent Control - Child lock (set the lock of the keyboard, only the RCU can control the TV)	No
Parent Control - Kid pass (preset the ontime, channel for each day of the week)	No
Parent Control - Channel lock (For digital transmission and DVD program, to filter some programms)	Yes
Calendar / Games	No
No program auto switch off	15 mins.
Hotel mode (Y/N)	T.B.D
DVD player (No/slot/tray)	No
Tuner FM (yes/No)	No
software download(RS232/CI/USB/OAD)	USB
Factory reset	Yes

Technical Specification

Screen saver	Yes
Blue Back	No
LED indicator(Power on/Standby)	Blue / Red
Connectors -Rear	
RF Input (Antenna): Air/ Cable/ 2in1	Air+Cable
Scart : CVBS in&out / RGB / S-VIDEO	No
CINCH video in / out（AV1）	No
CINCH audio in / out (No volumpe control on Audio out/can be jack 3,5mm)	No
S-video in	No
Component Video Input (YCrCb/YPrPb)	No
Component Audio Input (YCrCb/YPrPb)	No
VGA in / Audio L/R in / Jack audio in 3.5mm	VGA + dia. 3.5mm for audio in
HDMI	2
DVI	No
Audio input for DVI	No
CINCH subwoofer out / Coaxial out (S/PDIF)	No
Headphone output connector (mm)	No
CINCH subwoofer out / Coaxial out (S/PDIF)	S/PDIF out （Coaxial）
RS232 （Y/N , VGA or DB9 port …）	No
Card Readers	No
USB slot (No/1.1/2)	1 (Software update, JPEG, MP3, WMA, RMVB, DivX) Multimedia depends on license
DVB-CI (common interface)	No
External power converter input	No
Connectors -Side	
HDMI	1
AV-IN	1
AV-OUT	No
Component Video Input (YCrCb/YPrPb)	1
Component Audio Input (YCrCb/YPrPb)	1 (Share with AV audio in)
Headphone output connector (dia.mm)	1（3.5mm)
CINCH subwoofer out / Coaxial out (S/PDIF)	No
USB slot (No/1.1/2)	1 (Software update, JPEG, MP3, WMA, RMVB, DivX) Multimedia depends on license
DVB-CI (common interface)	No
DLNA	No
UI/RC	
UI design (font/pixel, 2D/3D graphic engine..)	SOD Standard
RC Model	YK76B3 (Toshiba code)
RC system	RGB Standard
RC # of keys	
Accessories included	
Carton (English/French/Spanish)	English

IB	English
Circuit diagram	No
Batteries	Yes
Product registration Card	Yes（English)
AC Cable Length	1.8m
Audio Cord (Jack 3.5mm)	No
VGA Cord	No
Wallmount frame	Optional
Antenna Cable	No
6 in 1(YPbPr & CVBS) cable adapter	No
3D Glasses	Yes (2 Sets)
General Data	
Size (W x H x D, with stand) in mm	-
Size (W x H x D, without stand) in mm	-
Package Size (W x H x D, without stand) in mm	-
Net Weight in kg	-
Gross Weight in Kg	-
Design / Mechanical	
Wallmount VESA compatible (standard reference)	Yes
Adaptor for VESA wallmount compatibility (accessory ref)	Yes
Desktop Stand (included/optionnal + ref/No)	included
Panel Tilt (Fowards/Backwards/Rotation)	No
Swivel function desktop stand (yes/No) + motorized?	No
Docking station (yes/No)	No
Floor Stand (included/optionnal + ref/No)	No
Glass shield (yes/No)	No
Finish on Front	-
Finish on side	-
Finish on back	-
Finish on stand	-
number of colors on carton box	2
Brand logo	Customer Inlet
Other logo	No
External AC/DC Power with DC power cord (yes/No)	No
Handle (yes/No)	No
Detachable speaker (yes/No)	No
Rating Label langages	English

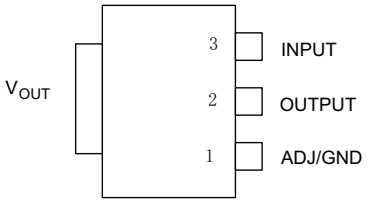

SYSTEM
POWER SUPPLY
KEY PAD, IR Receiver ,Ambient Sensor
Optional
PIXELWORKS 3D Processor
Motion Engine
PA131DG
FLASH
DDRII
DVB-T&ATV
Demo d
MSD309PX-LF-SB
DVB-T & IF Demo. Build in
MPEG1/2/4 /H.264 Decoder
JPEG MP3 Decoder
3D Comb filter Video Decoder
R/L
TPA3121
10W + 10W
Uplayer1
HDMI1
PR
PB
Y
R
L
Video
Side Terminals
DTV
ATV
Toshiba TC90517
ISDB-T Demod
SAW P/S
IF (ATV)
IF+/-
Rear Terminals
Uplayer2
HDMI2
HDMI3
PC
PC Audio
Tuner
S/PDIF

No.	Name	Position	Type	P/N
1	IR	U29	HS0038B4	5300-140038-0010
2	Speaker	Bass	SL-R3018H-3E	5600-106154-0060
		Treble	YDG3040-2	5600-708254-00
3	Crystal	Y2	49U3H	4900-125453-R000
		Y1	HC-49U/S	4900-124053-R000
4	Tuner	U10	VA1P1BF8405	5202-45733D-7H10
5	Saw	U30	F4401	4900-744015-0X00
6	IC	U3	MP1482DS	476A-M14820-0080
		U5	MP1482DS	476A-M14820-0080
		U50	MP1482DS	476A-M14820-0080
		U51	MP1482DS	476A-M14820-0080
		U9	W9751G6JB-25	4737-W97511-0840
		U15	W9751G6JB-25	4737-W97511-0840
		U24	EN25F32-100HIP	471R-N25321-0080
		U55	TC90517FG	4701-T90510-0640
		U37	AS1117L-3.3	47B6-A11170-03
		U38	AS1117L-3.3	47B6-A11170-03
		N1	AS1117L-3.3	47B6-A11170-03
		N2	AS1117L-1.2	47B6-A11175-0300
		U54	TPA3121D2PWPR	4722-T31210-0240
		U2	MSD309PX-LF-Z1-SB	475C-M30900-5230

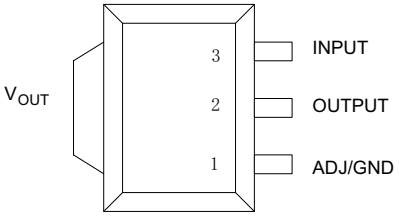
IC Block Diagram

Pin Configurations---AS1117L-3.3

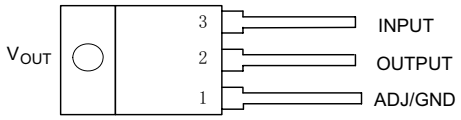
L Package
(SOT-223)



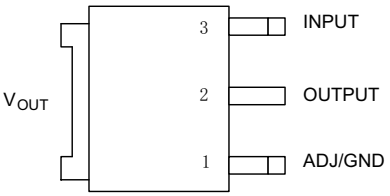
U Package
(SOT-89)



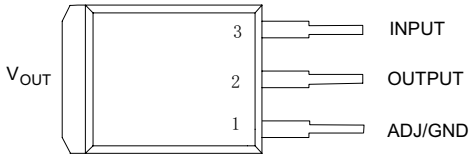
T Package
(TO-220)



R Package
(TO-252)

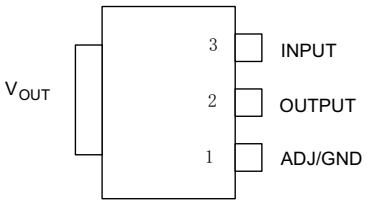


S Package
(TO-263)



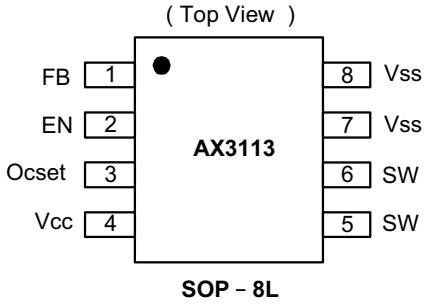
Pin Configurations---AS1117L-ADJ

L Package
(SOT-223)



❖ PIN ASSIGNMENT

The package of AX3113 is SOP-8L; the pin assignment is given by:



Name	Description
FB	Feedback pin
EN	Power-off pin H：normal operation(Step-down) L：Step-down operation stopped (All circuits deactivated)
OCSET	Add an external resistor to set max switch output current.
V_{CC}	IC power supply pin
SW	Switch pin. Connect external inductor & diode here.
V_{SS}	GND pin

LM4558

SOIC-8/DIP-8

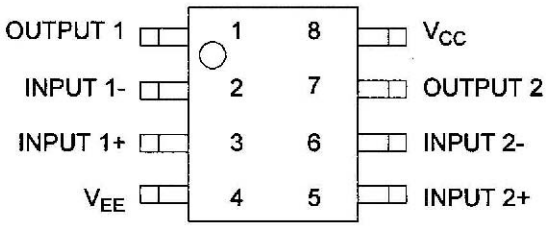
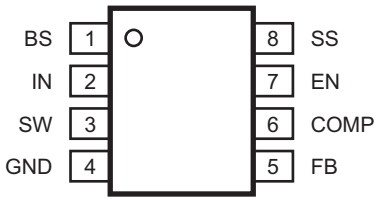


Figure 2. Pin Configuration of LM4558 (Top View)

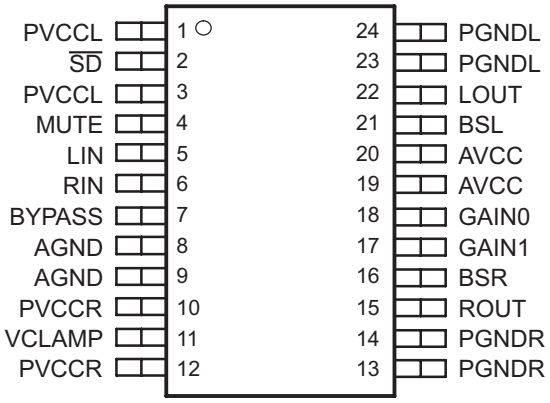
MP1482DS

TOP VIEW

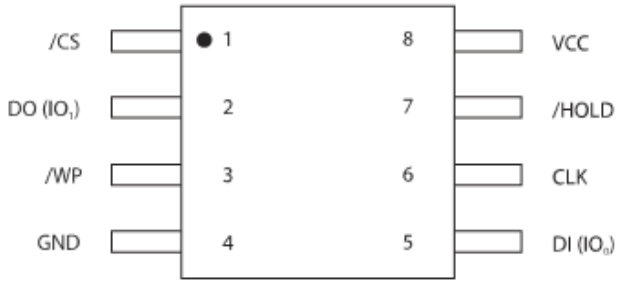


W25X40BVSNIG

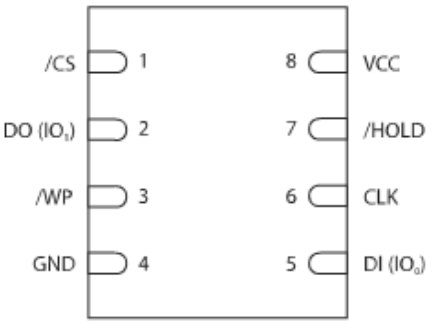
PWP (TSSOP) PACKAGE
(TOP VIEW)



PIN CONFIGURATION
SOIC 150-MIL / 208-MIL



PAD CONFIGURATION
WSON 6X5-MM



PIN CONFIGURATION
PDIP 300-MIL

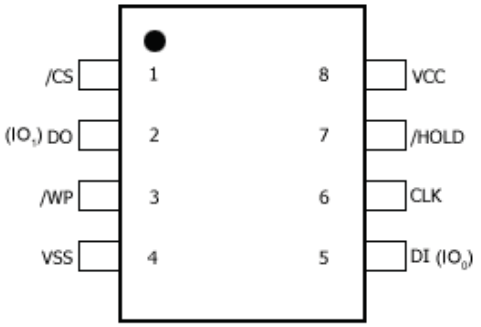
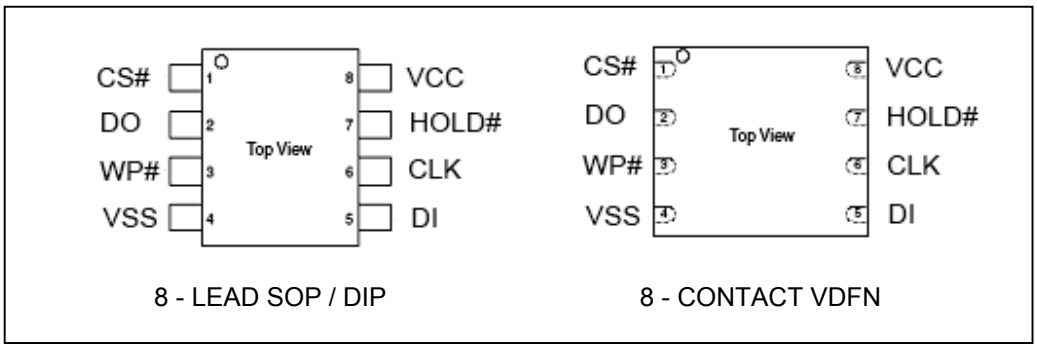
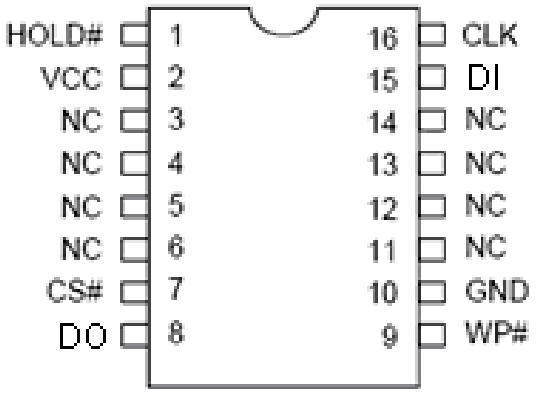


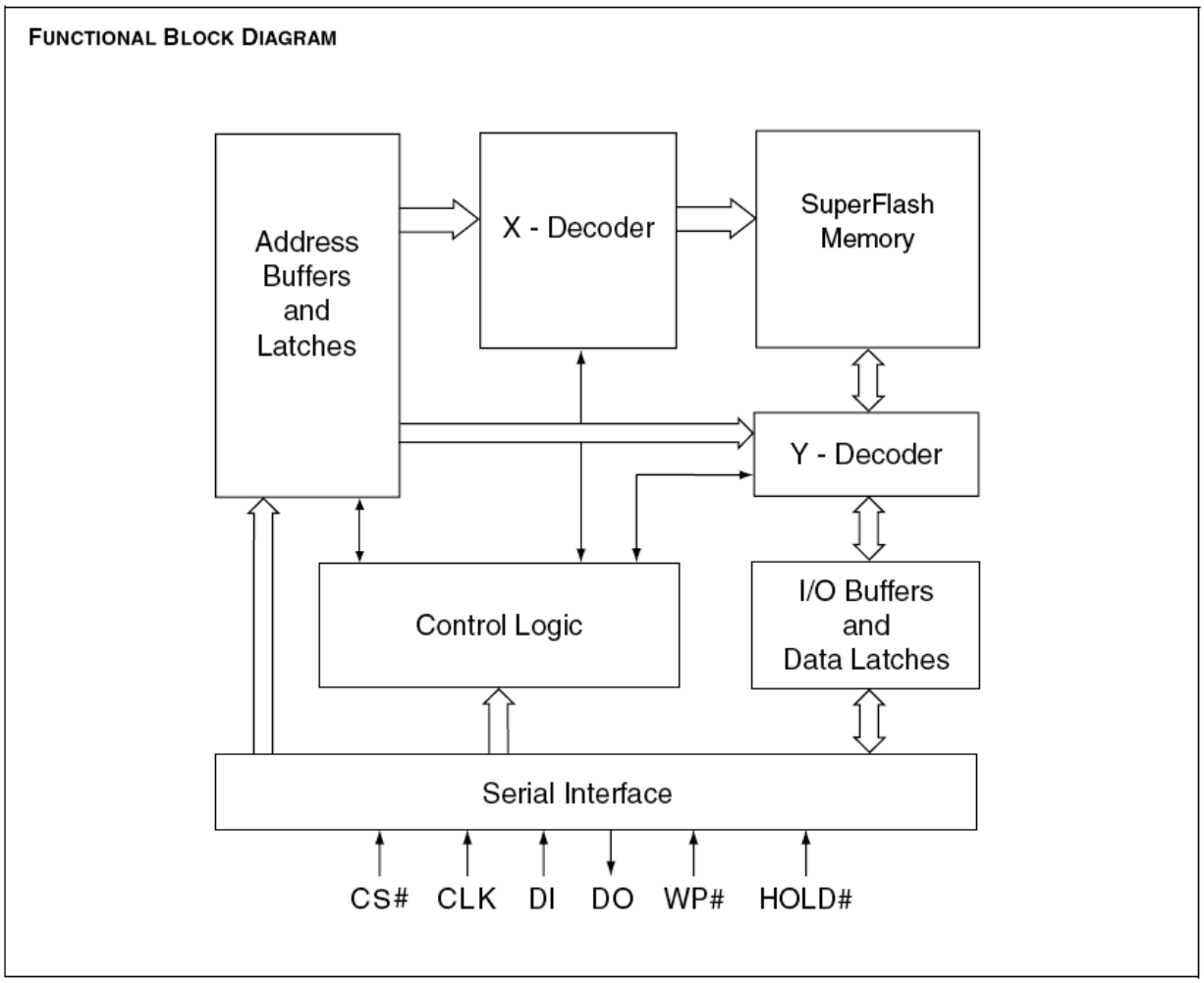
Figure.1 CONNECTION DIAGRAMS





16 - LEAD SOP

Figure 2. BLOCK DIAGRAM



SIGNAL DESCRIPTION

Serial Data Input (DI)
The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin.

Serial Data Output (DO)
The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

Serial Clock (CLK)
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)
The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Hold (HOLD#)
The HOLD pin allows the device to be paused while it is actively selected. When HOLD is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). The hold function can be useful when multiple devices are sharing the same SPI signals.

Write Protect (WP#)
The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1and BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.

Table 1. PIN Names

Symbol	Pin Name
CLK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
CS#	Chip Enable
WP#	Write Protect
HOLD#	Hold Input
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground

2. Configuration

All functions required for ISDB-T demodulation and error correction are built into the TC90517.
The input signals to be supported are a low IF (intermediate frequency) signal and direct IF signal. Baseband IQ signals can also be input.

The output signal is an MPEG-2 transport stream (TS) in serial format. Note that a TS in parallel format can be output by setting registers.

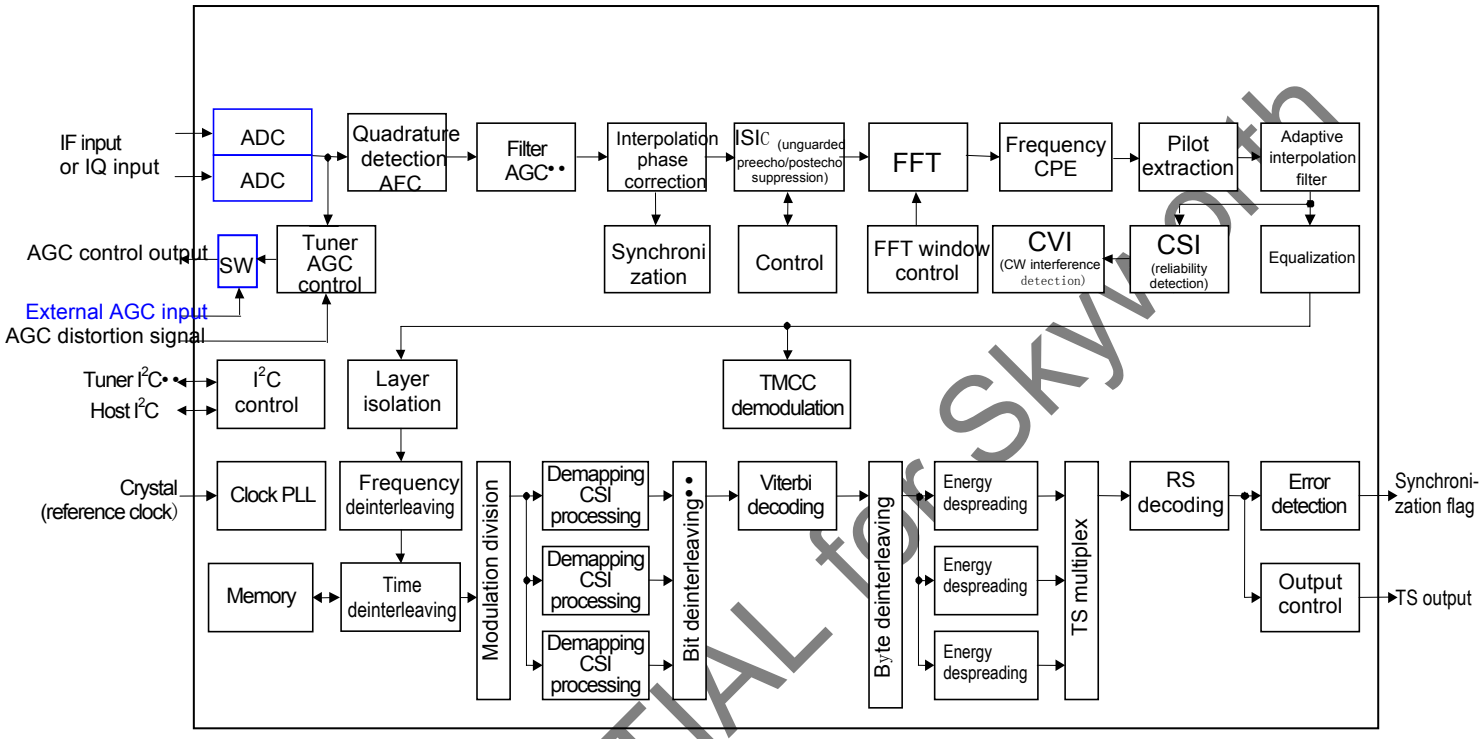
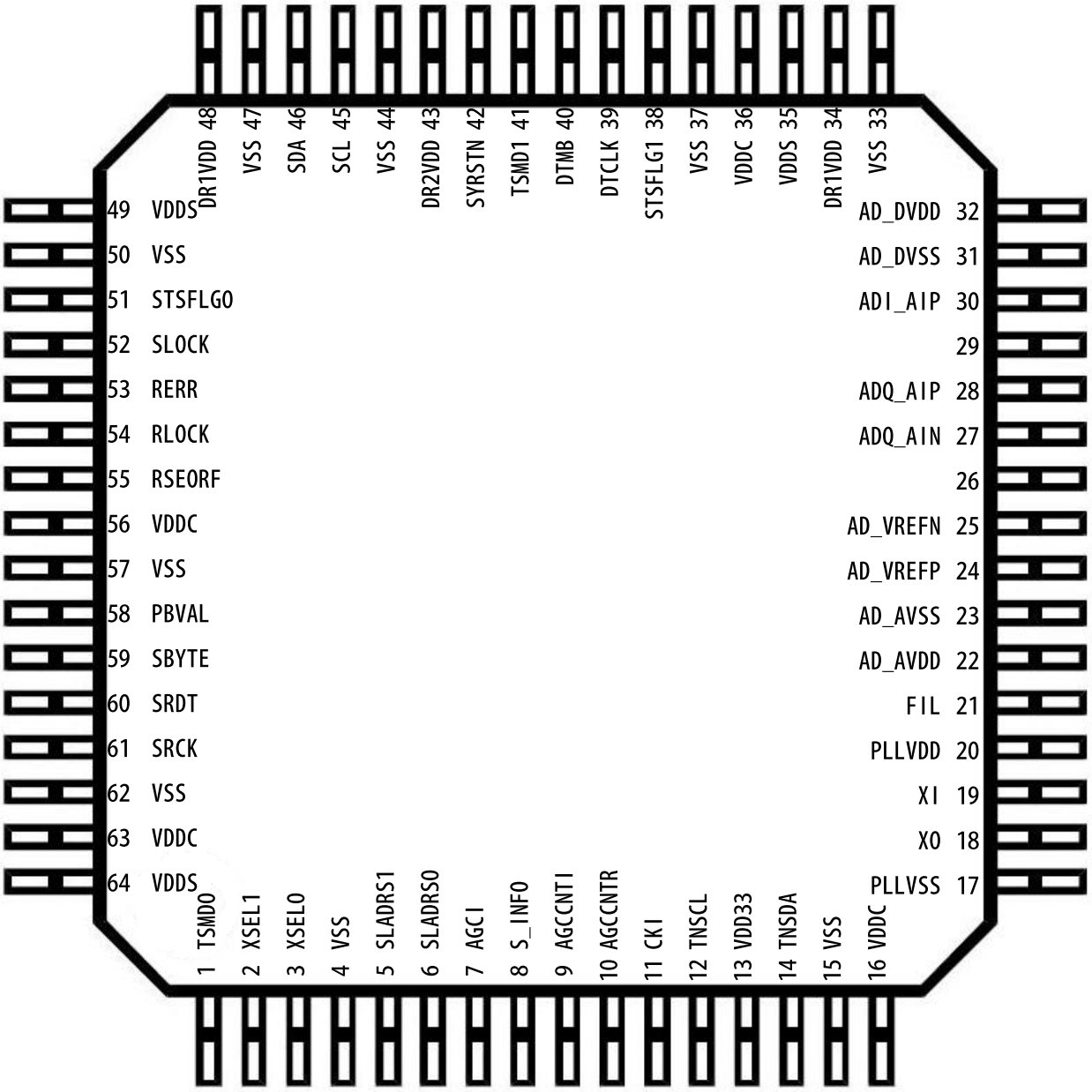


Fig. 2.1 TC90517FG Block Diagram

3. Pin Assignment (Top view)



4. Pin Functions

This specification indicates pins and their signals in upper case letters and registers and their signals in lower case letters.

Pin	Pin name	(Note4) I/O	(Note5,7) PU/PD	Function(Note 3)	Remarks(Note 2 and 6)
1	TSMDO	I	–	Shut down	0: Normal operation 1: Shut down
2	XSEL1	I	-	Crystal frequency division ratio 1	Set according to crystal frequency.
3	XSEL0	I	-	Crystal frequency division ratio 0	Set according to crystal frequency.
4	VSS	-	-	Digital GND	Connects to DGND.
5	SLADRS1	I/O	-	Slave address 1	Set according to slave address.
6	SLADRS0	I/O	-	Slave address 0	Set according to slave address.
7	AGCI	I	-	External AGC input	Connects to DGND when not used.
8	S_INFO	I	-	Pin for pre-shipment test	Connects to DGND.
9	AGCCNTI	I/O	PD	IF_AGC control output	Connects to tuner IF_AGC control input pin.
10	AGCCNTR	I/O	PD	RF_AGC control output	Connects to tuner RF_AGC control input pin. Open, fixed to L when not used.
11	CKI	I	-	Pin for pre-shipment test	Connects to DGND.
12	TNSCL	I/O	OD	I2C clock output	Connects to tuner I2C clock pin. (Pull-up performed outside IC.)
13	VDDS	-	-	I/O power supply	Connects to digital +3.3 V typ.
14	TNSDA	I/O	OD	I2C data I/O	Connects to tuner I2C data pin. (Pull-up performed outside IC.)
15	VSS	-	-	Digital GND	Connects to DGND.
16	VDDC	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
17	PLLVSS	-	-	Clock PLL GND	Connects to AGND.
18	XO	O	-	Crystal output	Connects to crystal. ixosl="1" and open when an external reference clock is input.
19	XI	I	–	Crystal or reference clock input	Connects to crystal. The amplitude (p-p) is 0.5 V to PLLVDD when an external reference clock is input.
20	PLLVDD	-	-	Clock PLL power supply	Connects to analog +2.5 V typ.
21	FIL	O	-	PLL filter output	Connects to AGND via 1500 pF.
22	AD_AVDD	-	-	ADC analog power supply	Connects to analog +2.5 V typ.
23	AD_AVSS	-	-	ADC analog GND	Connects to AGND.
24	AD_VREFP	-	-	ADC reference voltage output	+1.75 V typ. Connects to AGND via PC.
25	AD_VREFN	-	-	ADC reference voltage output	+0.75 V typ. Connects to AGND via PC.
26	AD_VREF	-	-	ADC reference voltage output	+1.25 V typ. Connects to AGND via PC.
27	ADQ_AIN	I	-	Q signal (differential negative side) input	Single-ended IF: Connects to AGND via PC. Differential IF: Connects to AGND via PC. Single-ended IQ: Connects to AGND via PC. Differential IQ: Connects to tuner Q (-) output after the DC component was cut.
28	ADQ_AIP	I	-	Q signal (differential positive side) input	Single-ended IF: Connects to AGND via PC. Differential IF: Connects to AGND via PC. Single-ended IQ: Connects to tuner Q output after the DC component was cut. Differential IQ: Connects to tuner Q (+) output after the DC component was cut.
29	ADI_AIN	I	-	IF signal (differential negative side) input or I signal (differential negative side) input	Single-ended IF: Connects to AGND via PC. Differential IF: Connects to tuner IF (-) output after the DC component was cut. Single-ended IQ: Connects to AGND via PC. Differential IQ: Connects to tuner I (-) output after the DC component was cut.
30	ADI_AIP	I	-	IF signal (differential positive side) input or I signal (differential positive side) input	Single-ended IF: Connects to tuner IF output after the DC component was cut. Differential IF: Connects to tuner IF (+) output after the DC component was cut. Single-ended IQ: Connects to tuner I output after the DC component was cut. Differential IQ: Connects to tuner I (+) output after the

					DC component was cut.
31	AD_DVSS	-	-	ADC digital GND	Connects to DGND.
32	AD_ DVDD	-	-	ADC digital power supply	Connects to digital +2.5 V typ.
33	VSS	-	-	Digital GND	Connects to DGND.
34	DR1VDD	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
35	VDDS	-	-	I/O power supply	Con nects to digital +3.3 V typ.
36	VDDC	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
37	VSS	-	-	Digital GND	Connects to DGND.
38	STSFLG1	O	PD	Status flag 1 output	Open, fixed to L when not used.
39	DTCLK	I	PD	Pin for pre-shipment test	Open or connects to DGND.
40	DTMB	I	PU	Pin for pre-shipment test	Open or connects to digital +3.3 V typ.
41	TSMD1	I	-	Pin for pre-shipment test	Connects to DGND.
42	SYRSTN	I/O	OD	System reset input	Inputat specified timing at power ON.
43	DR2VDD	-	-	Digital +2.5 V power supply	Connects to digital +2.5 V typ.
44	VSS	-	-	Digital GND	Connects to DGND.
45	SCL	I/O	OD	I2C clock input for host CPU	Connects to I2C clock bus. (Pull-up performed outside IC.)
46	SDA	I/O	OD	I2C data I/O for host CPU	Connects to I2C data bus. (Pull-up performed outside IC.)
47	VSS	-	-	Digital GND	Connects to DGND.
48	DR1VDD	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
49	VDDS	-	-	I/O power supply	Con nects to digital +3.3 V typ.
50	VSS	-	-	Digital GND	Connects to DGND.
51	STSFLG0	I/O	PD	Status flag 0 output	Open, fixed to L when not used.
52	SLOCK	O		Synchronization completion (sequence 8 or higher) flag	Open, fixed to L when not used.
53	RERR	O	-	RS decoding error flag output	Open, fixed to L when not used.
54	RLOCK	O	-	RS decoding error free flag output	Open, fixed to L when not used.
55	RSEORF	O	-	TS error flag output	Open, fixed to L when not used.
56	VDDC	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
57	VSS	-	-	Digital GND	Connects to DGND.
58	PBVAL	O	-	TS valid flag output	Open, fixed to L when not used.
59	SBYTE	O	-	TS synchronization byte flag output	Open, fixed to L when not used.
60	SRDT	O	-	Serial TS data output	-
61	SRCK	O	-	TS serial clock output	-
62	VSS	-	-	Digital GND	Connects to DGND.
63	VDDC	-	-	Digital +1.2 V power supply	Connects to digital +1.2 V typ.
64	VDDS	-	-	I/O power supply	Con nects to digital +3.3 V typ.

Note 2 AGND is the abbreviation for analog GND, and DGND is the abbreviation for digital GND.

Note 3 The test dedicated pin is used for the pre-shipment test only. Make sure that processing is performed as indicated in the "Remarks" column. Any other method will lead to malfunction or failure.

Note 4 I/O indicates the type of the cell used. It may be different from the pin function because a test is conducted concurrently.

Note 5 PU indicates an I/O with a pull-up resistor (50 k☒typ.) and PD indicates an I/O with a pull-down resistor (50 k☒typ.). Pulling down the PU pin or pulling up the PD pin outside the IC sometimes changes the electric potential to the midpoint, resulting in instability. Caution is required.

Note 6 The unused output pins must be open and fixed to L by setting the output enable control register of each pin for noise reduction or to the output OFF state.

Note 7 OD indicates an open drain I/O. To use the pin for output, pull up the resistance outside the IC.

* The following pins are added with the upgrade from TC90507 to TC90517 (except the changes of power supply and GND pins):

Pin Number	Pin Name	Description
21	FIL	Added to the PLL loop filter.
27	ADQ_AIN	Added for IQ input (differential).
28	ADQ_AIP	Added for IQ input.
7	AGCI	Added to passthrough the AGC control signal of other ICs.
52	SLOCK	Changed from conventional FLOCK.

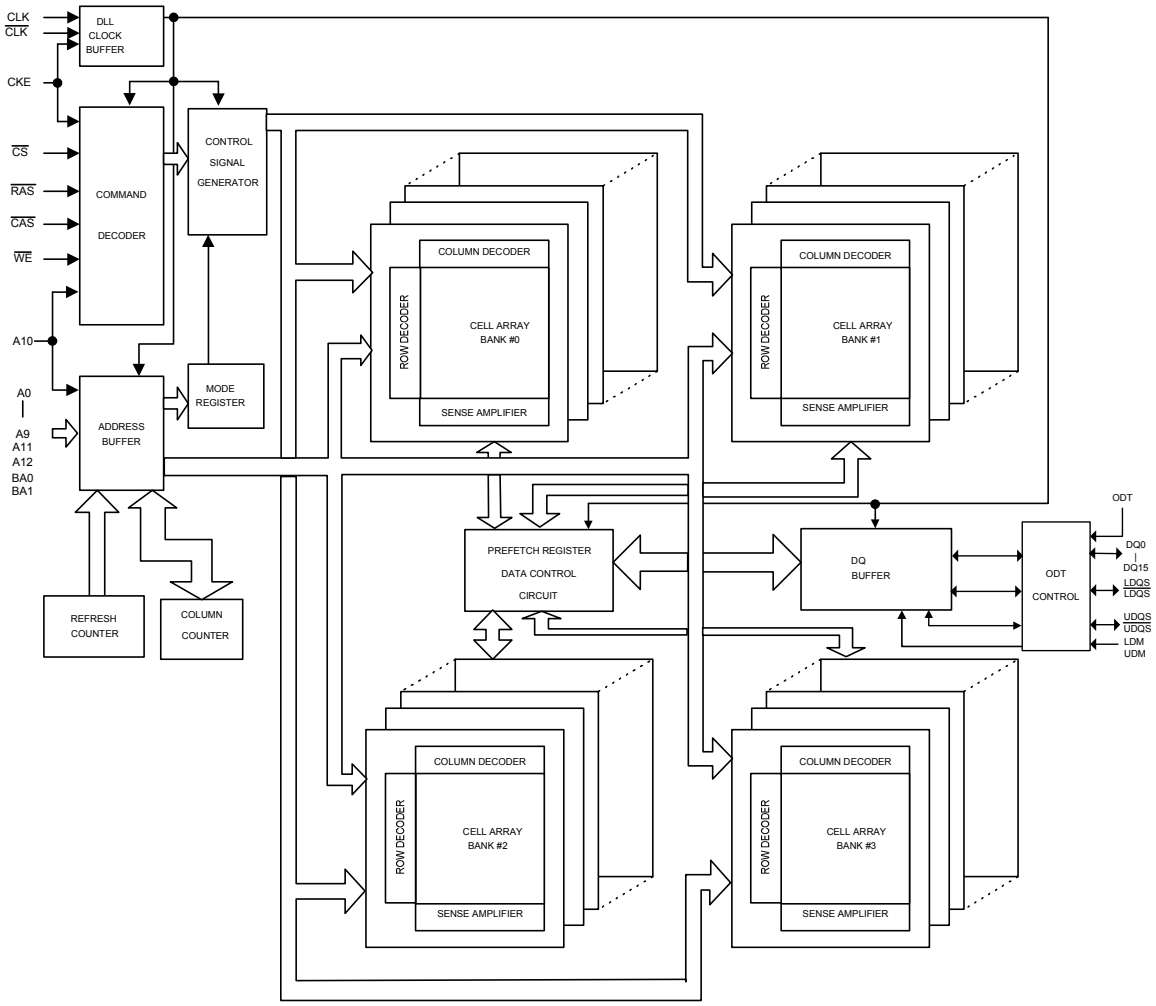
4. BALL CONFIGURATION

1	2	3	4	5	6	7	8	9
VDD	NC	VSS		A		VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM		B		UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ		C		VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11		D		DQ10	VSSQ	DQ13
VDD	NC	VSS		E		VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM		F		LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ		G		VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3		H		DQ2	VSSQ	DQ5
VDDL	VREF	VSS		J		VSSDL	CLK	VDD
	CKE	$\overline{\text{WE}}$		K		$\overline{\text{RAS}}$	$\overline{\text{CLK}}$	ODT
NC	BA0	BA1		L		$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1		M		A2	A0	VDD
VSS	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	VSS
VDD	A12	NC		R		NC	NC	

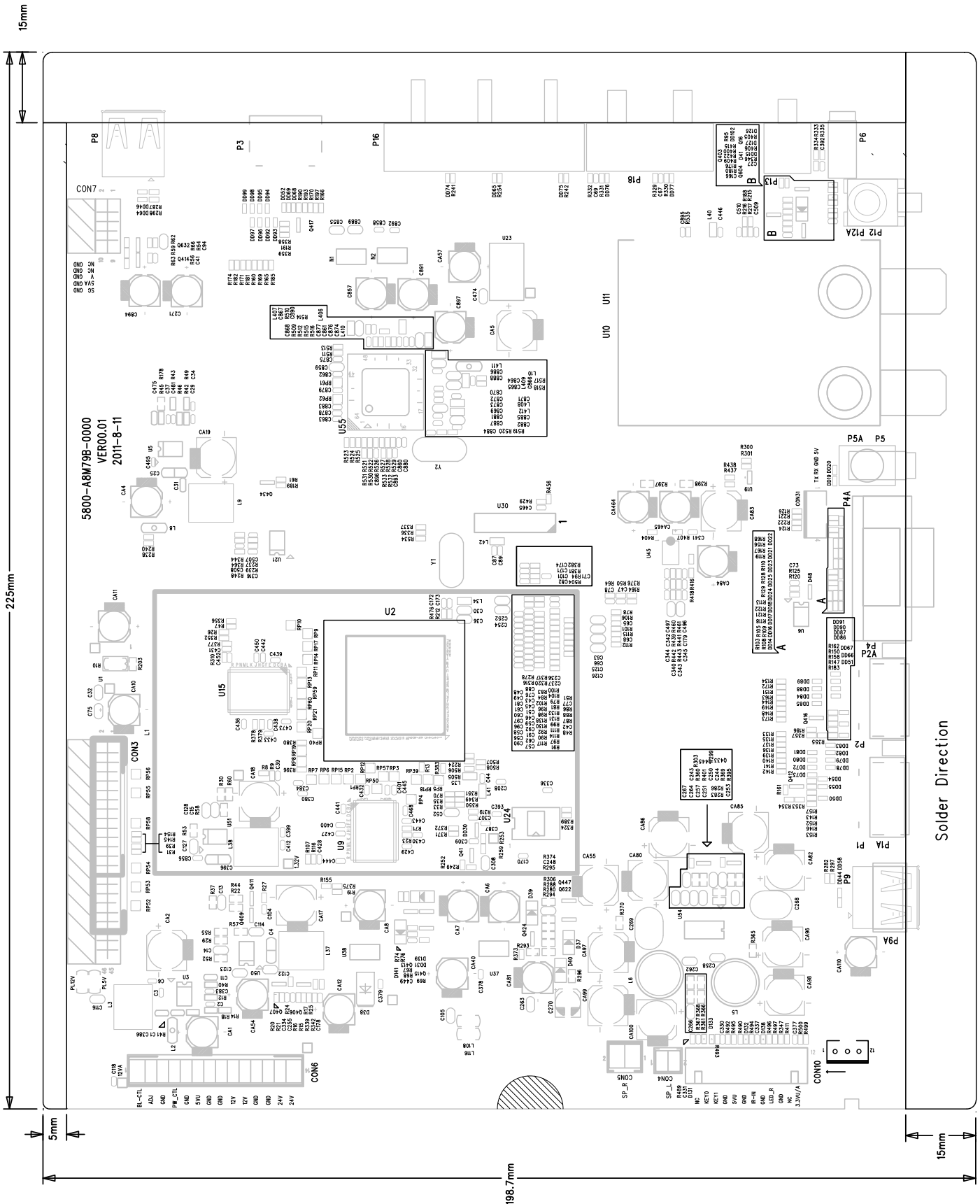
5. BALL DESCRIPTION

BALL NUMBER	SYMBOL	FUNCTION	DESCRIPTION
M8,M3,M7,N2,N8,N3,N7,P2,P8,P3,M2,P7,R2	A0–A12	Address	Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. Row address: A0–A12. Column address: A0–A9. (A10 is used for Auto-precharge)
L2,L3	BA0–BA1	Bank Select	BA0–BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
G8,G2,H7,H3,H1,H9,F1,F9,C8,C2,D7,D3,D1,D9,B1,B9	DQ0–DQ15	Data Input / Output	Bi-directional data bus.
K9	ODT	On Die Termination Control	ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM.
F7,E8	LDQS, $\overline{\text{LDQS}}$	LOW Data Strobe	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS corresponds to the data on DQ0–DQ7. $\overline{\text{LDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
B7,A8	UDQS, $\overline{\text{UDQS}}$	UP Data Strobe	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS corresponds to the data on DQ8–DQ15. $\overline{\text{UDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
L8	$\overline{\text{CS}}$	Chip Select	All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external bank selection on systems with multiple ranks. $\overline{\text{CS}}$ is considered part of the command code.
K7,L7,K3	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Command Inputs	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
B3,F3	UDM LDM	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
J8,K8	CLK, $\overline{\text{CLK}}$	Differential Clock Inputs	CLK and $\overline{\text{CLK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{\text{CLK}}$. Output (read) data is referenced to the crossings of CLK and $\overline{\text{CLK}}$ (both directions of crossing).
K2	CKE	Clock Enable	CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
J2	V_{REF}	Reference Voltage	V_{REF} is reference voltage for inputs.
A1,E1,J9,M9,R1	V_{DD}	Power Supply	Power Supply: 1.8V ± 0.1V.
A3,E3,J3,N1,P9	V_{SS}	Ground	Ground.
A9,C1,C3,C7,C9,E9,G1,G3,G7,G9	V_{DDQ}	DQ Power Supply	DQ Power Supply: 1.8V ± 0.1V.
A7,B2,B8,D2,D8,E7,F2,F8,H2,H8	V_{SSQ}	DQ Ground	DQ Ground. Isolated on the device for improved noise immunity.
A2,E2,L1,R3,R7,R8	NC	No Connection	No connection.
J7	V_{SSDL}	DLL Ground	DLL Ground.
J1	V_{DDL}	DLL Power Supply	DLL Power Supply: 1.8V ± 0.1V.

6. BLOCK DIAGRAM



NOTE: The cell array configuration is 8192 * 1024 * 16


15mm
225mm
5mm
198.7mm
15mm
5800-A8M79B-0000
VER00.01
2011-8-11
Solder Direction
P8
P3
P16
P18
P13
P12
P12A
P6
P5A
P5
P4A
P4
P2A
P2
P1A
P1
P9A
P9
CON7
CON3
CON6
CON10
U2
U9
U10
U11
U15
U23
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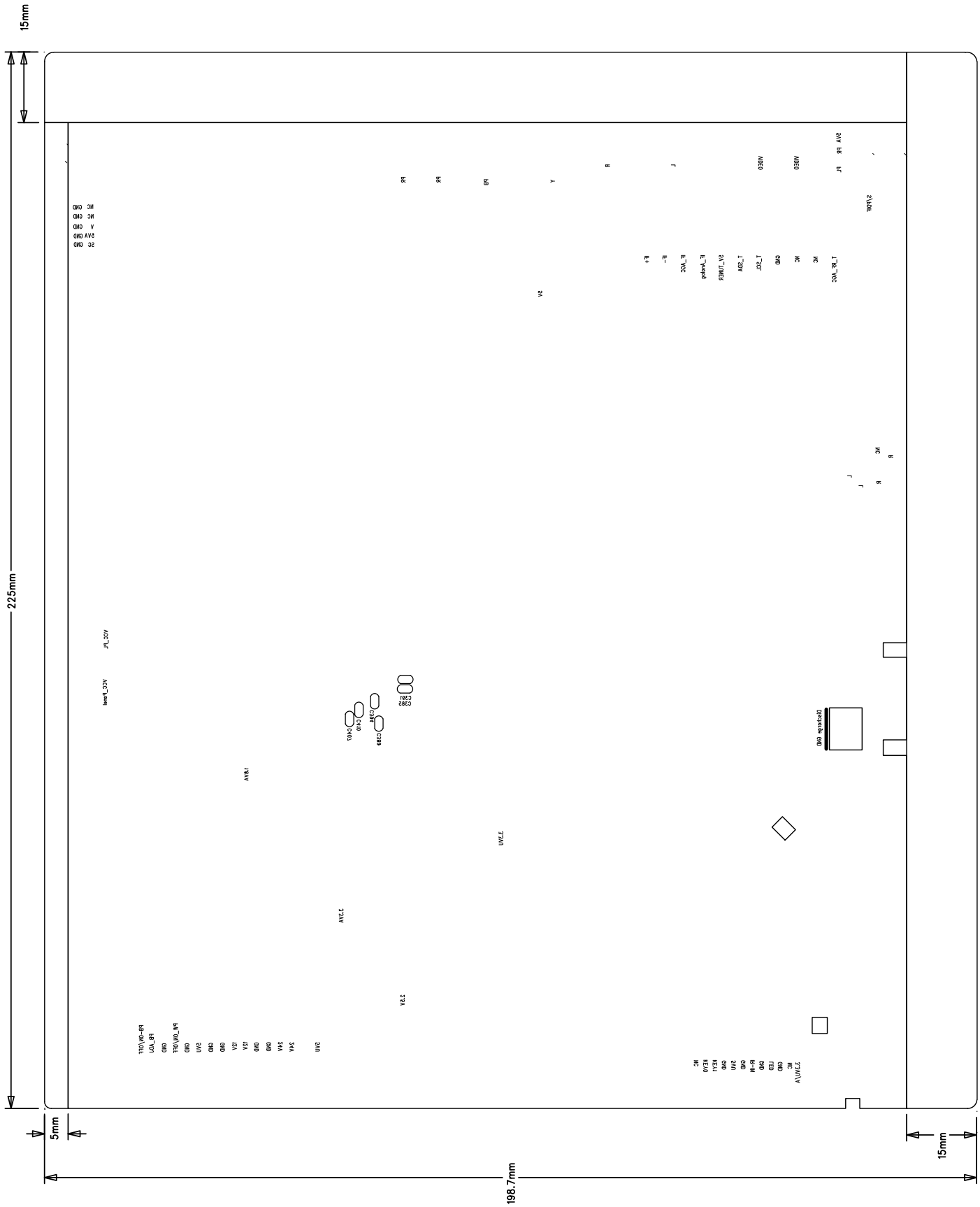
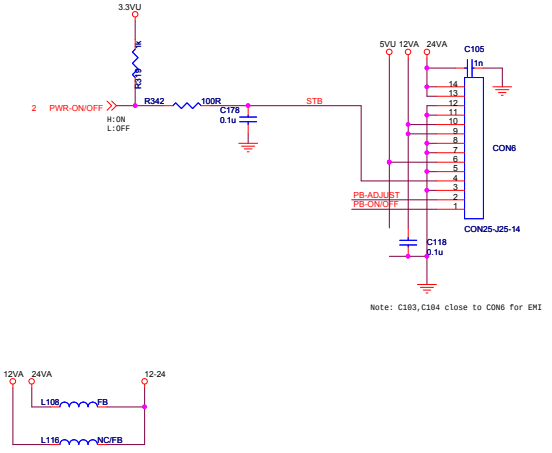
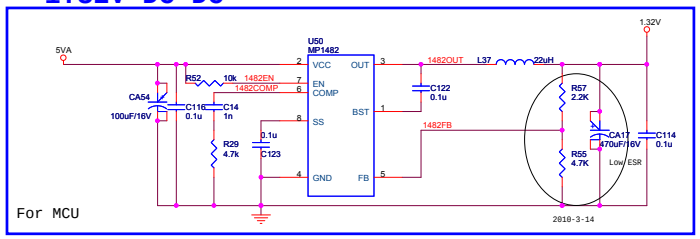
CONN5
CONN6
CONN7
CONN8
CONN9
CONN10


15mm
225mm
5mm
198.7mm
15mm

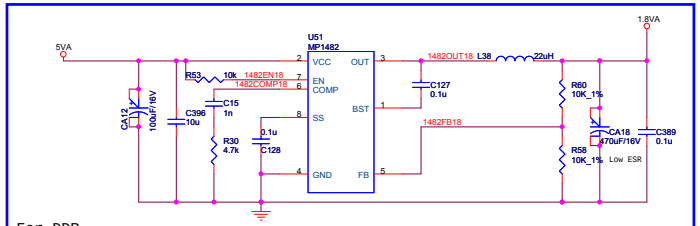
Power Input



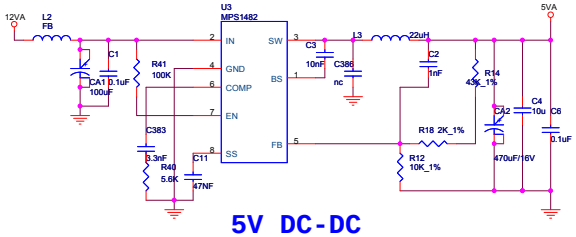
1.32V DC-DC



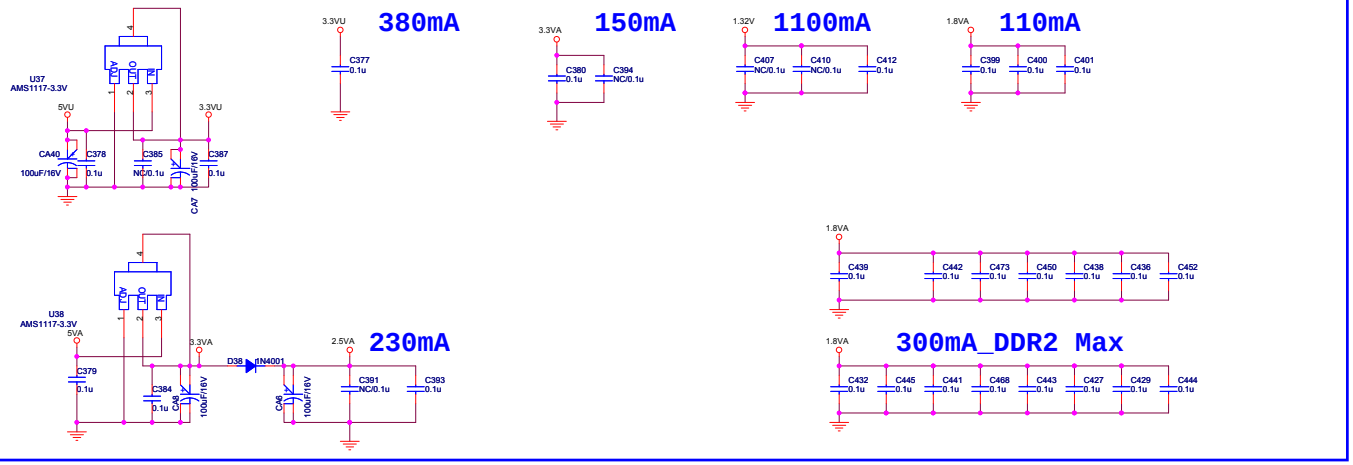
1.8V DC-DC



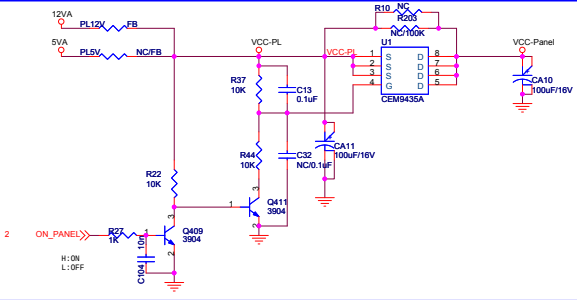
DC-DC Module



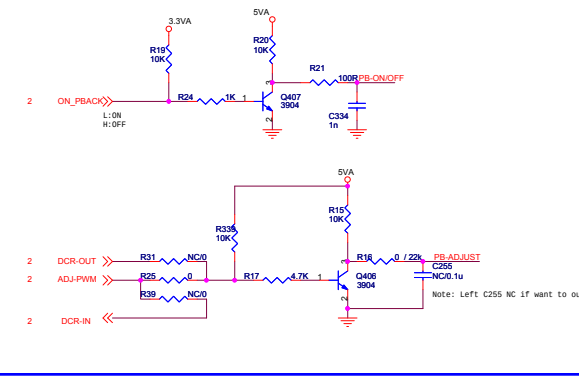
MST Power supply



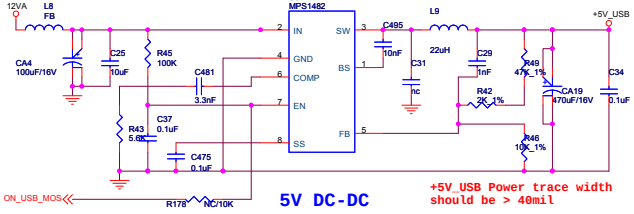
PANEL POWER



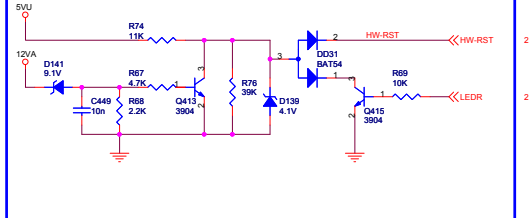
Inverter Interface



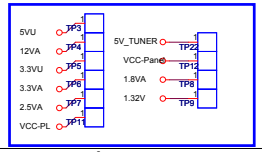
USB Power



For Power Drop



Power Test Point



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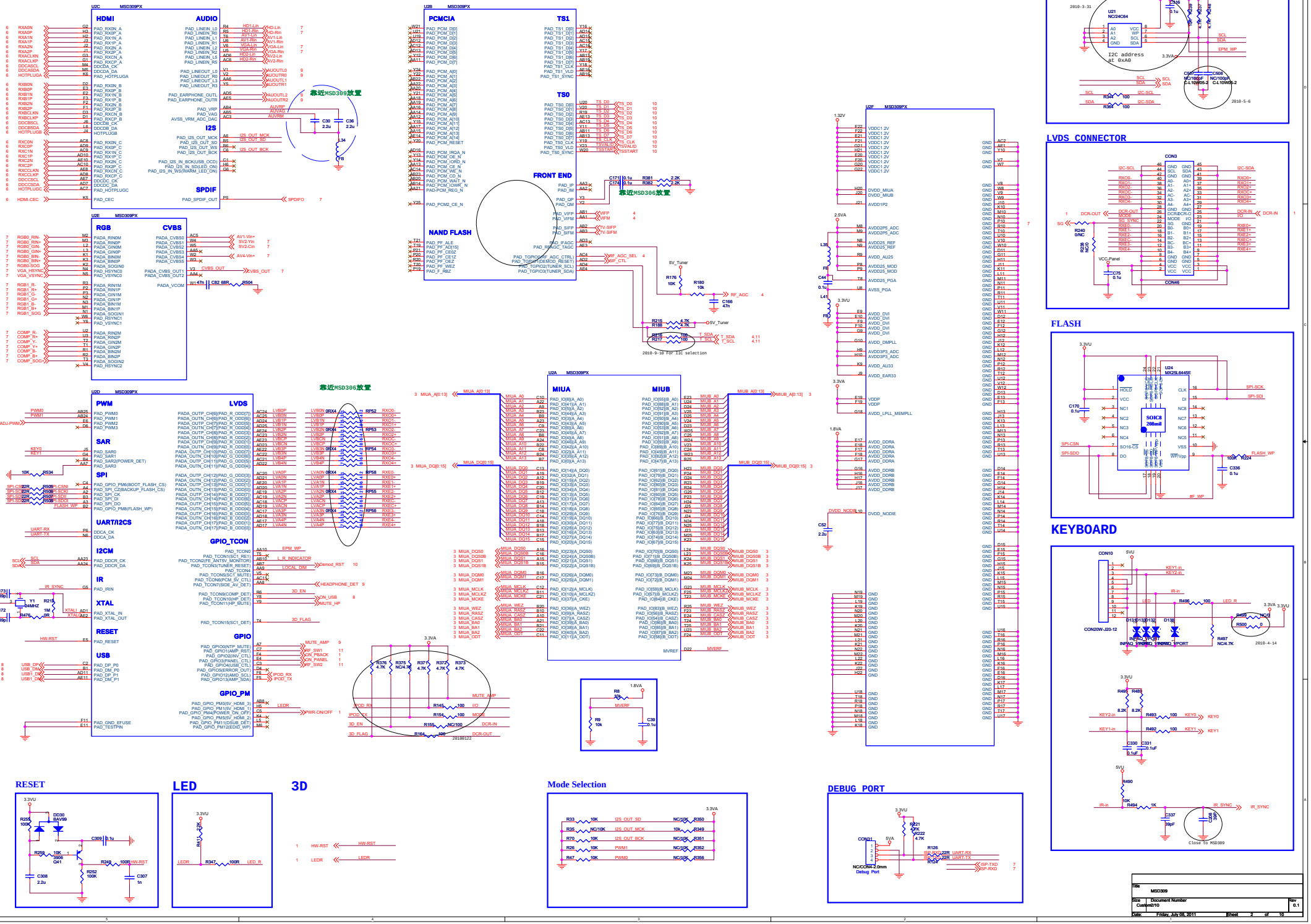

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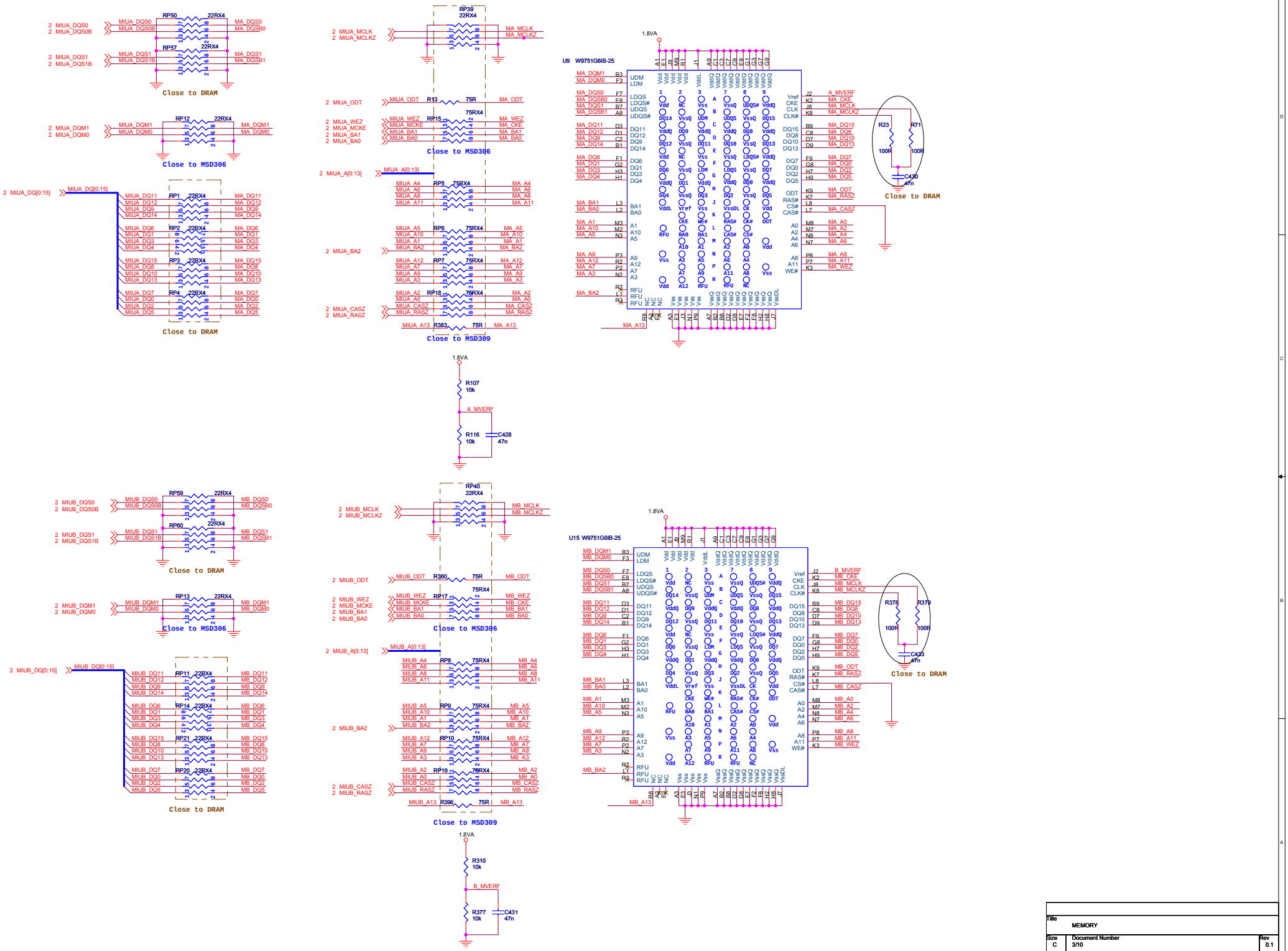

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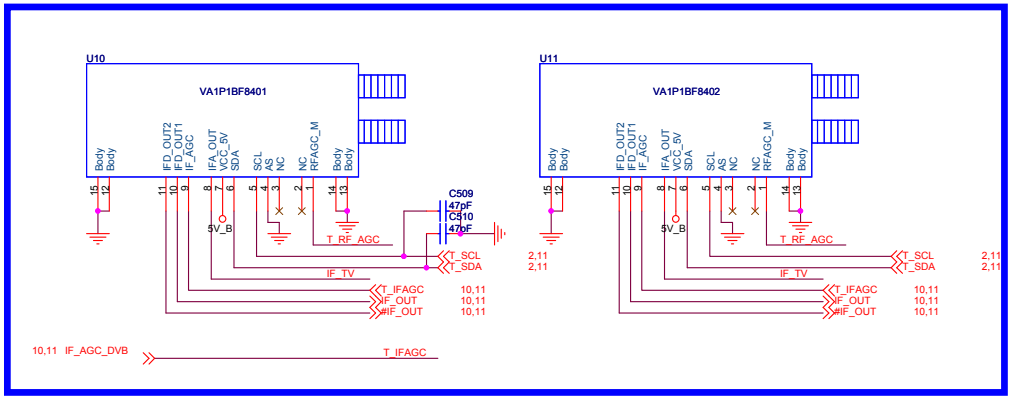
ISDB-T TUNER



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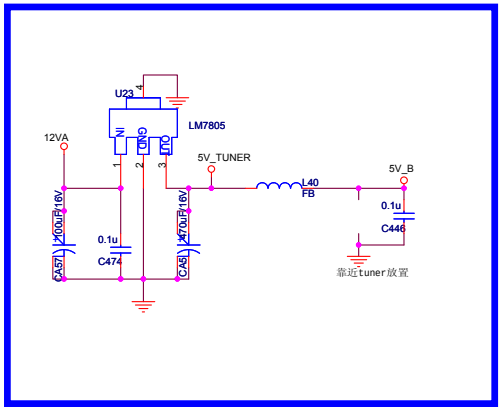

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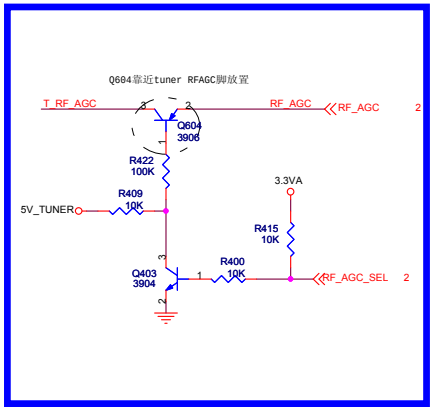

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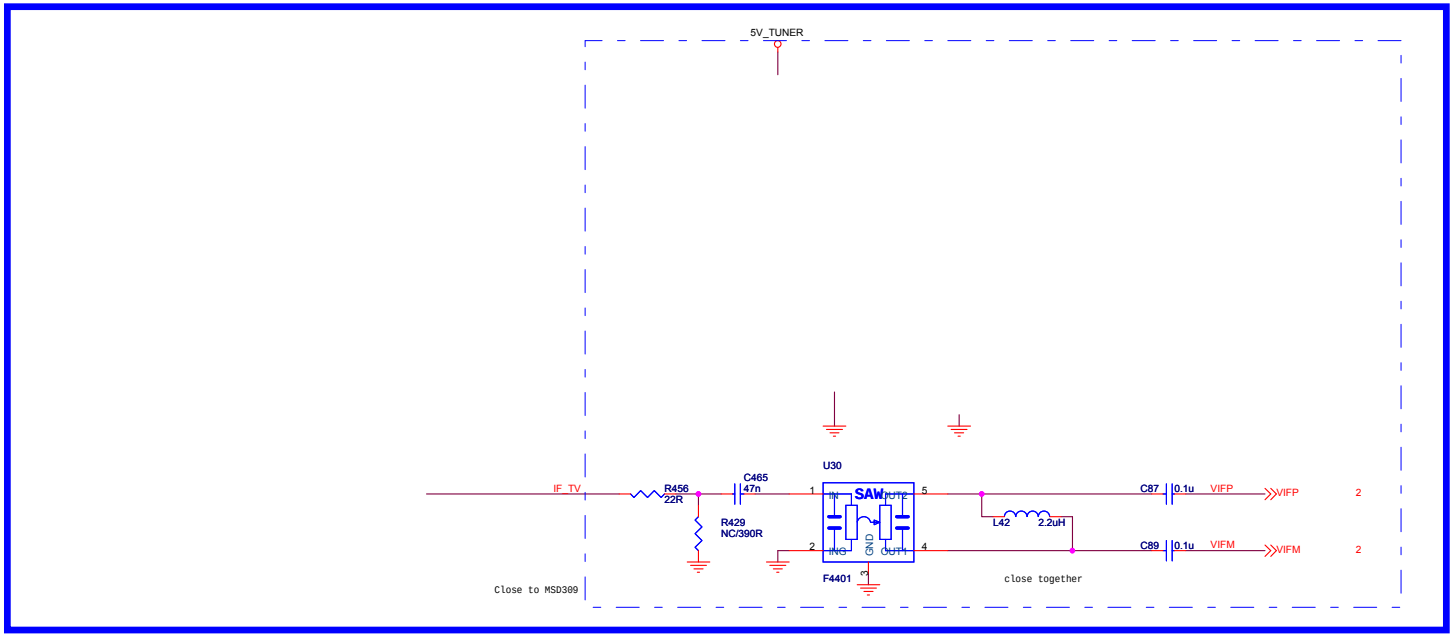

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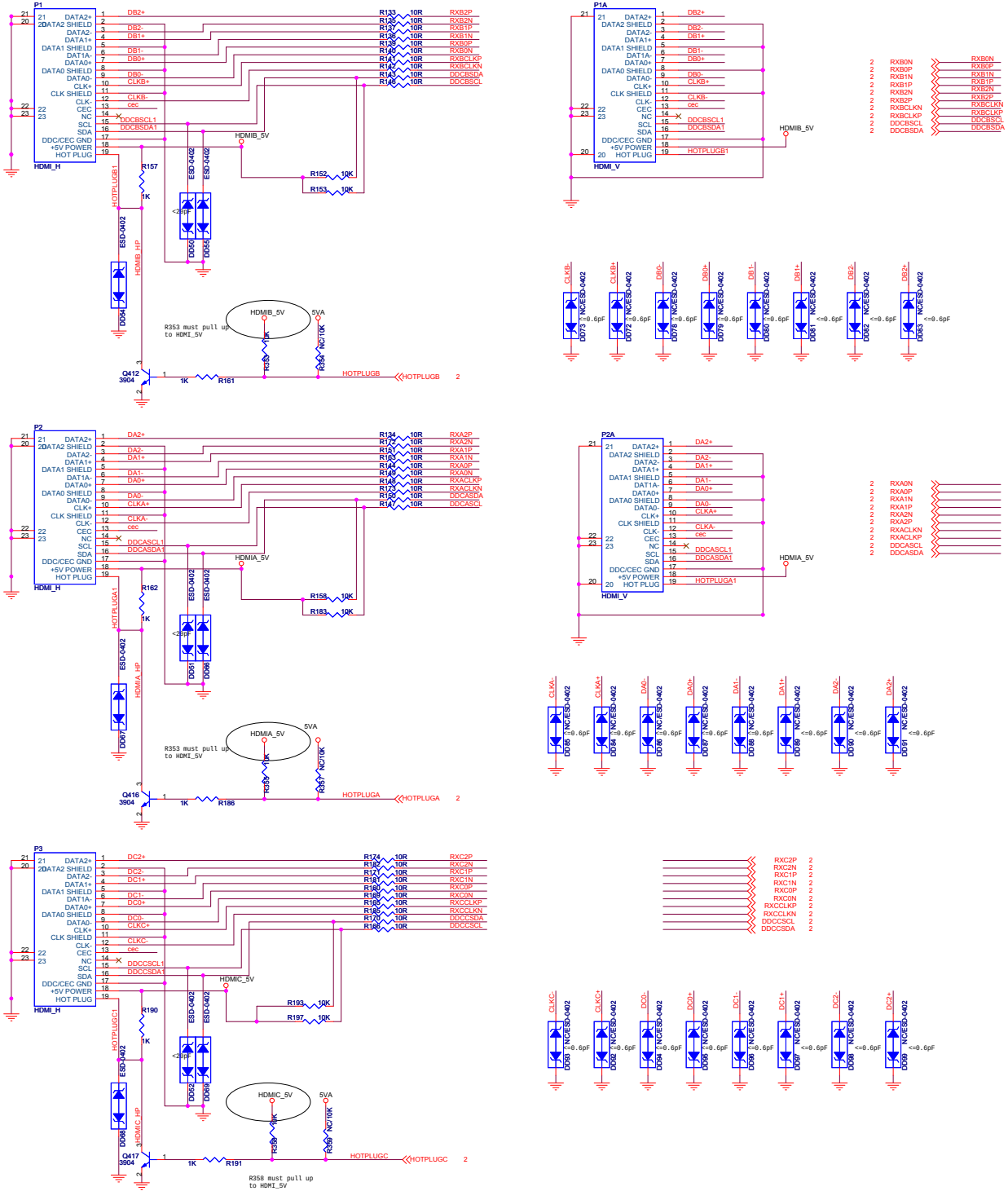
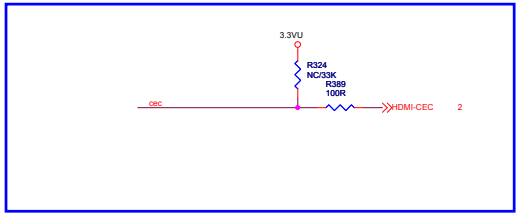


HDMI CEC



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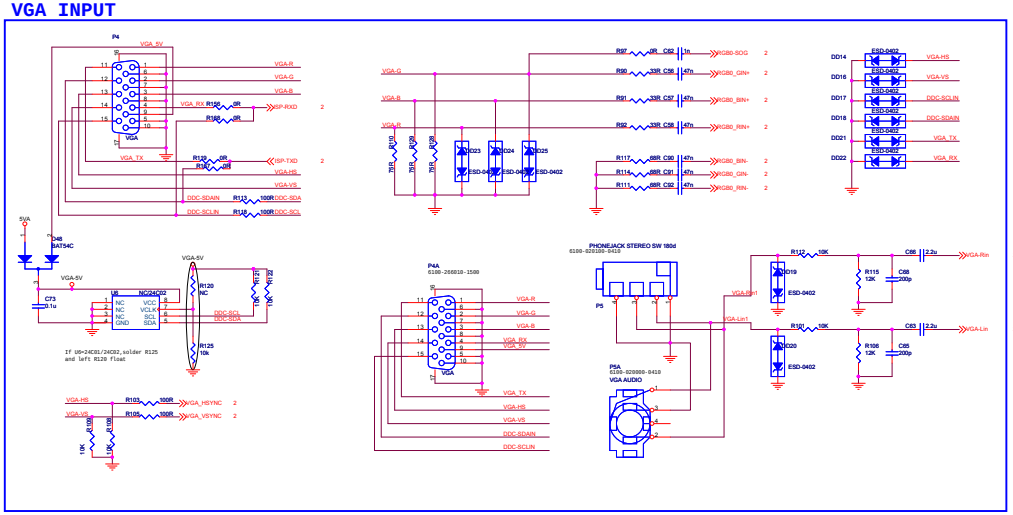

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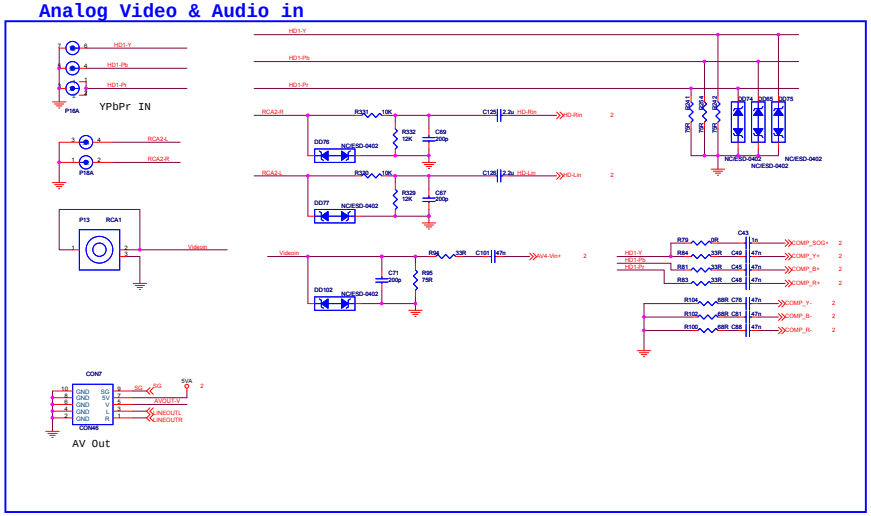

FOR UN-USED PORTS

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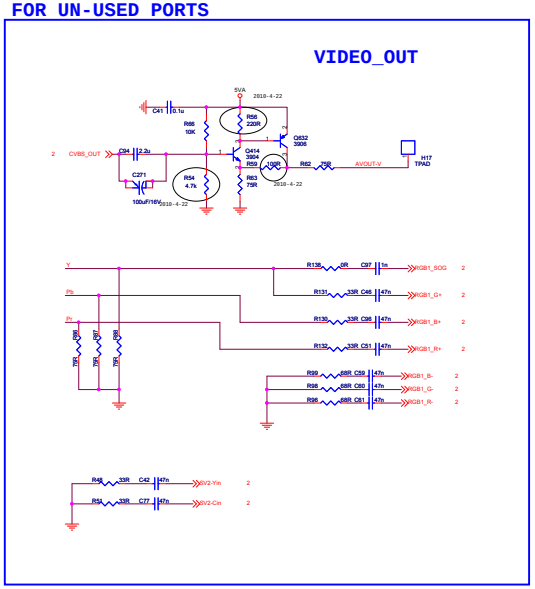
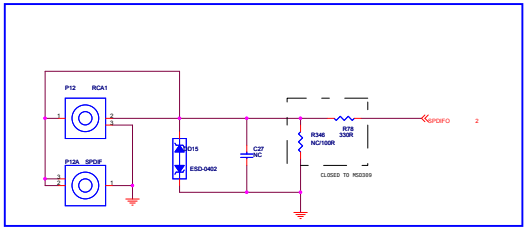


SPDIF_Coaxial Out



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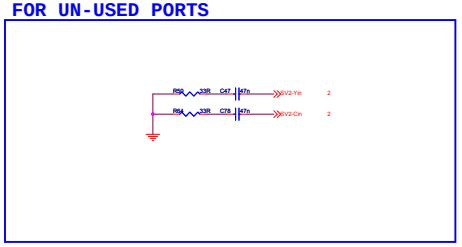

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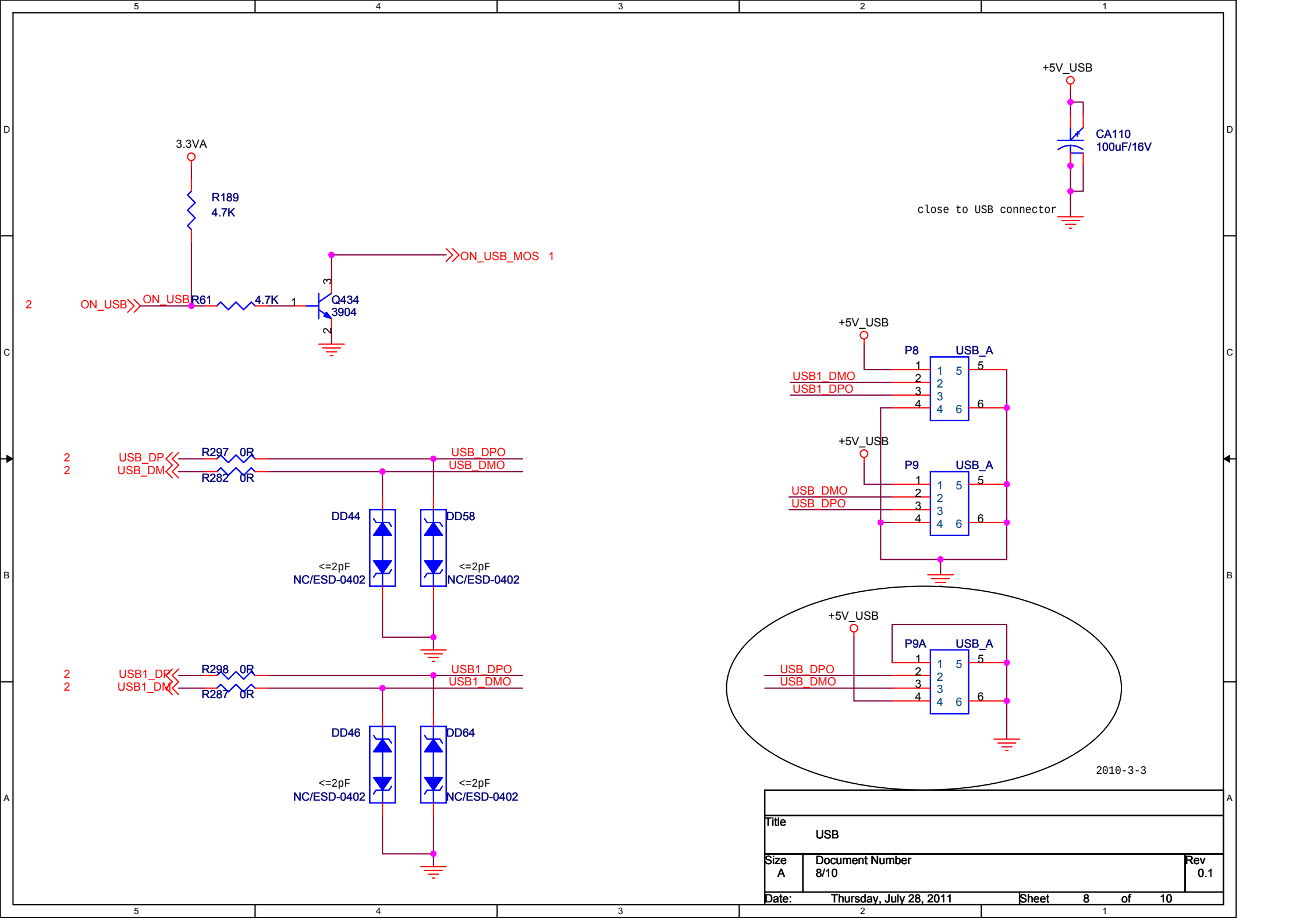
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2
ON_USB
ON_USB
R61
4.7K
1
Q434
3904
3
2
+5V_USB
CA110
100uF/16V
close to USB connector
2
USB_DP
2
USB_DM
R297 0R
R282 0R
USB_DPO
USB_DMO
DD44
DD58
<=2pF
NC/ESD-0402
<=2pF
NC/ESD-0402
2
USB1_DP
2
USB1_DM
R298 0R
R287 0R
USB1_DPO
USB1_DMO
DD46
DD64
<=2pF
NC/ESD-0402
<=2pF
NC/ESD-0402
+5V_USB
P8
USB_A
USB1_DMO
USB1_DPO
+5V_USB
P9
USB_A
USB_DMO
USB_DPO
+5V_USB
P9A
USB_A
USB_DPO
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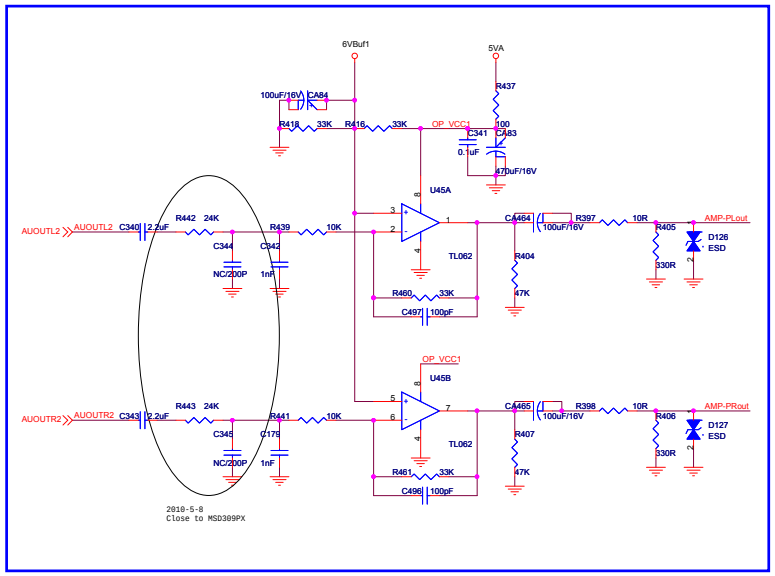

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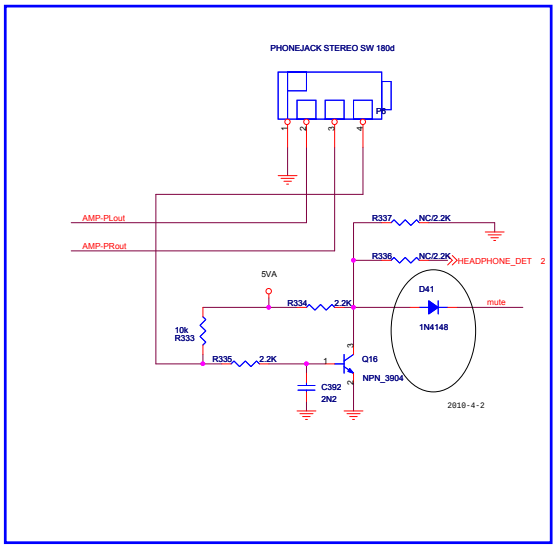
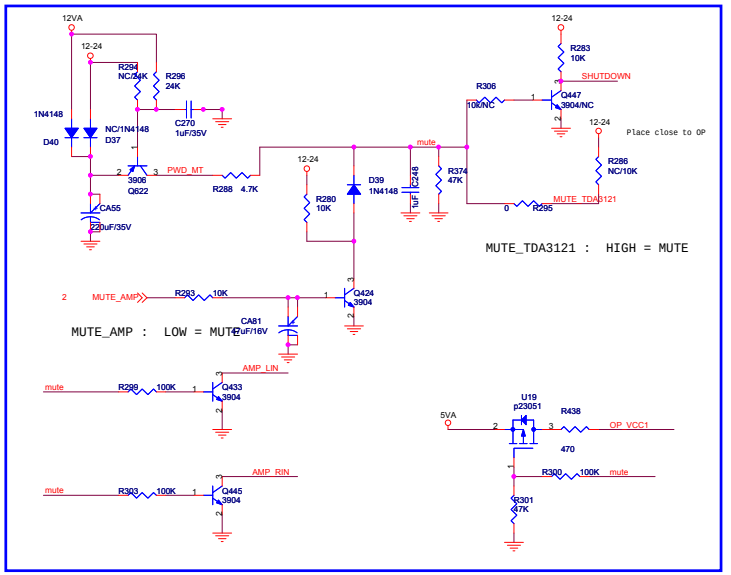
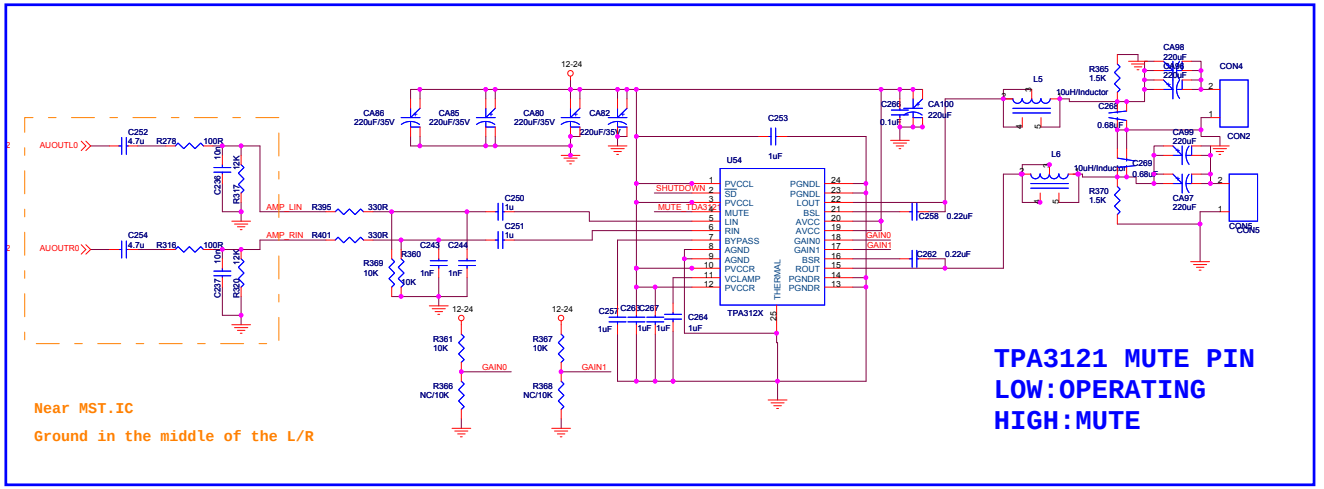


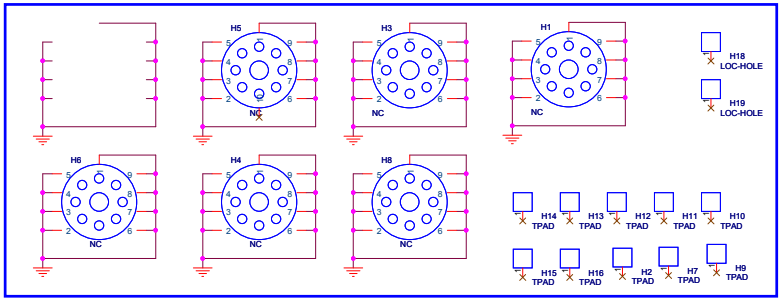
Power Down MUTE

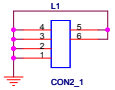


TDA3121



HOLE





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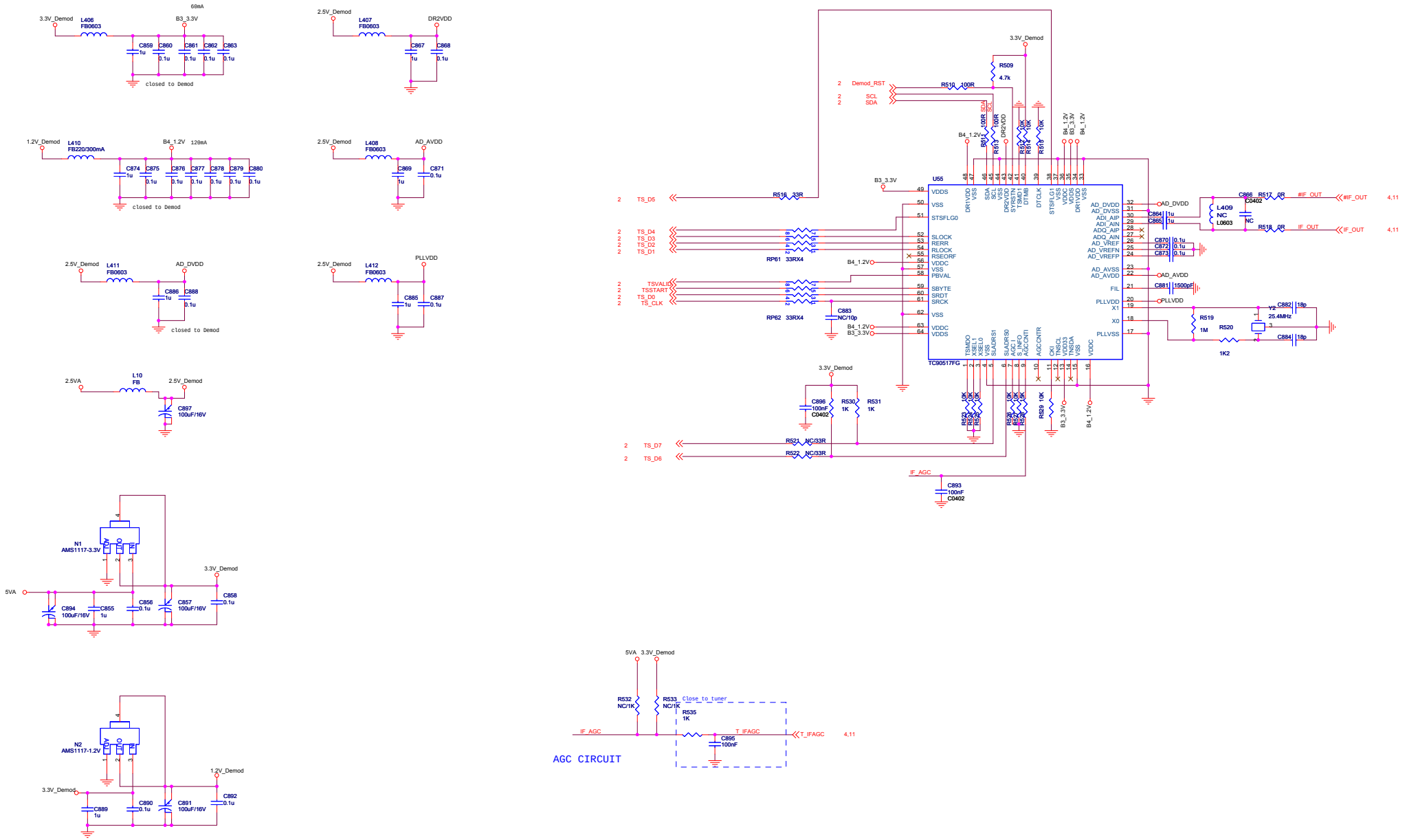

MStar semiconductor

ISDB-TC90517FG

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Skyworth
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SKYWORTH R&D CENTER

Power Supply Service Manual

PART NO. : 168P-P32EWM-K0

DESCRIPTION :

VERSION NO. : 1.0

PAGE : 13

DESCRIBED : Zhou Cong

CHECKED : Hu xiangfeng

APPROVED : Bao xiaojie

Released Date: 2012-07-21

Modification record

Edition	Modification date	Record	Described	Checked	Approved
1.0	2012-7-21	First record	Zhou Cong	Hu Xiangfeng	Bao Xiaojie

Contents

Warning

This manual is only used for the experienced service person , and does not apply to the general consumer。The manual does not have warnning or alert for the potential hazards caused of the non-technical personnel attempting to repair this product . Electrical products should be an experienced professional and technical personnel for maintenance and repair ,any other person attempts to maintain and repair the products covered by this manual will likely be seriously hurt or even life-threatening.

1. General Description

1.1 General description of power supply

This power apply to 32-inch universal standard power interface; the total standby power consumption less than 1W (5V DC the Load 50mA); protection functions; low cost; mature power supply structure; the voltage range is 90-264V and wide supply voltage input,. For 32" LED panel, supplies 4 channels, each channel nominal current value is 130mA。

1.2 Main technical specifications

1.2.1 Input Electrical Characteristics

Input voltage range	90Vac to 264Vac
Rated voltage range	100Vac to 240Vac
Frequency range	50Hz/60Hz±5%
Max input ac current	0.85Amax at 100Vac input & full load condition
Inrush current (cold start)	70Atyp peak
Efficiency(full load)	80%min @ 100Vac, Full Load
Harmonic current	Meet GB17625.1-1998/IEC61000-3-2 class D
Leakage Current	Less Than 0.75mA, 230Vac input
Standby Power Loss	≦1W, 240Vac input, 50mA Load of 5V
Input Fuse	T3.15A L/250Vac

1.2.2 Output Electrical Characteristics

Output Voltage	Regulation	Min. current	Rated current	Peak current
+24V	+24V±5%	0.1A	2.0A	2.5A
+12V	+12V±5%	0.1A	2.0A	3.0A
+5VSB	+5V±5%	0.1A	0.5A	0.8A

Note:* pulse width within 100ms .

1.2.3 Output ripple and noise

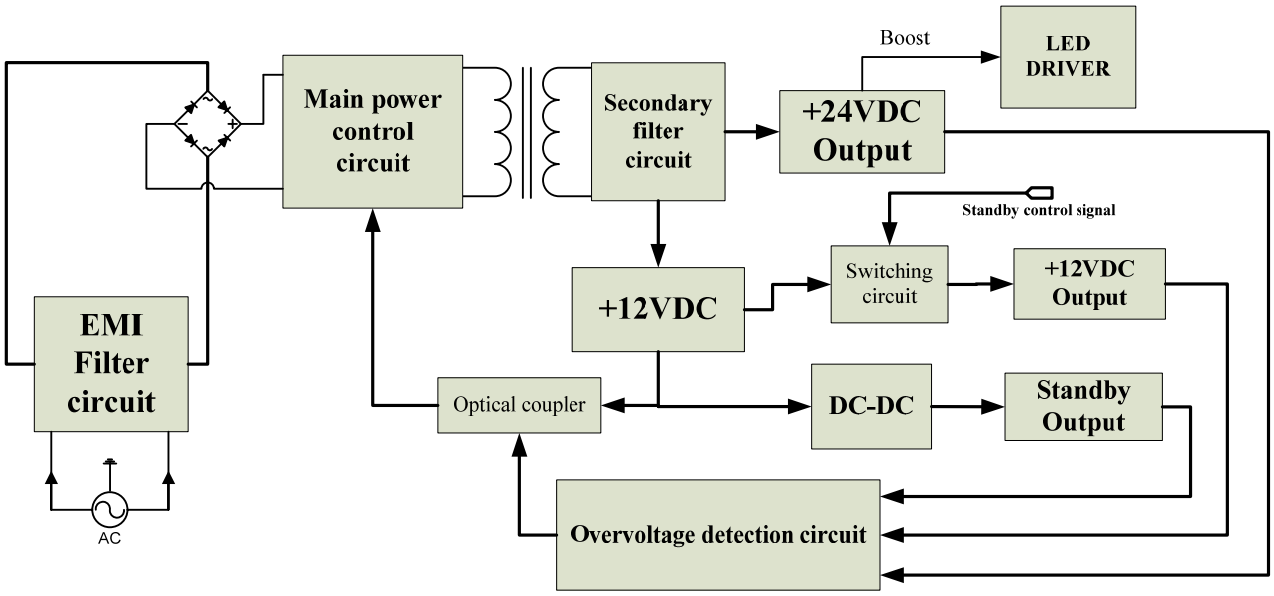
Output Voltage	Ripple & Noise (Max.)
+24V	240mVp-p@25℃; 350mVp-p@-10℃
+12V	120mVp-p@25℃; 200mVp-p@-10℃
+5VSB	100mVp-p@25℃; 200mVp-p@-10℃

Note: 1) Measurements shall be made with an oscilloscope with 20MHz bandwidth.

2) Outputs shall be bypassed at the connector with a 0.1uF ceramic capacitor and a 10uF electrolytic capacitor to simulate system loading.

2. Circuit description

2. 1 The power circuit diagram



2. 2 Each part of the circuit description

2. 2. 1 the main part of the circuit：NXP TEA1733P

Features

- SMPS controller IC enabling low-cost applications
- Large input voltage range (12 V to 30 V)
- Very low supply current during start-up and restart (typically 10 μA)
- Low supply current during normal operation (typically 0.5 mA without load)
- Overpower or high/low line compensation
- Adjustable overpower time-out
- Adjustable overpower restart timer
- Fixed switching frequency with frequency jitter to reduce EMI
- Frequency reduction with fixed minimum peak current to maintain high-efficiency at low output power levels
- Slope compensation for CCM operation
- Low and adjustable OverCurrent Protection (OCP) trip level
- Adjustable soft start operation

2.2.2 the LED driver of the circuit：MICRO ELECTRONICS OZ9967

VIN – Input Voltage		6.0V – 33V
Maximum Operating Junction Temp.		125 °C
COMP 1~ 6, ISW		≤40V
VREF, ENA, STATUS		0.0V to 5.5V
OVP, DIM, SSTCMP, CT, LCT, DRV, TIMER, RANGLED, UVLS, ISEN 1~6		0.0V to VREF
Operating Frequency		100kHz - 1MHz
LED Current per String		10mA – 350mA
PWM Frequency		100Hz – 10kHz
R_{CT}		> 20kohm
OZ9967 Operating Temperature[3]		-20 °C to +85 °C
OZ9967I Operating Temperature[3]		-40 °C to +85 °C
Operating Junction Temperature[3]		125 °C
Thermal Impedance[3,4]	θ_{J-C}	θ_{J-A}
28 pin SSOP	15°C/W	78°C/W
28 pin TSSOP	8°C/W	70°C/W
28-pin SOP	10 °C/W	64 °C/W

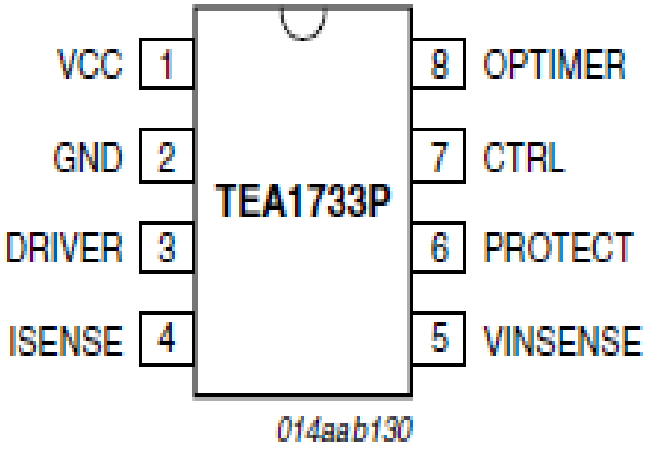
3. The main chip description

3.1 The main chip

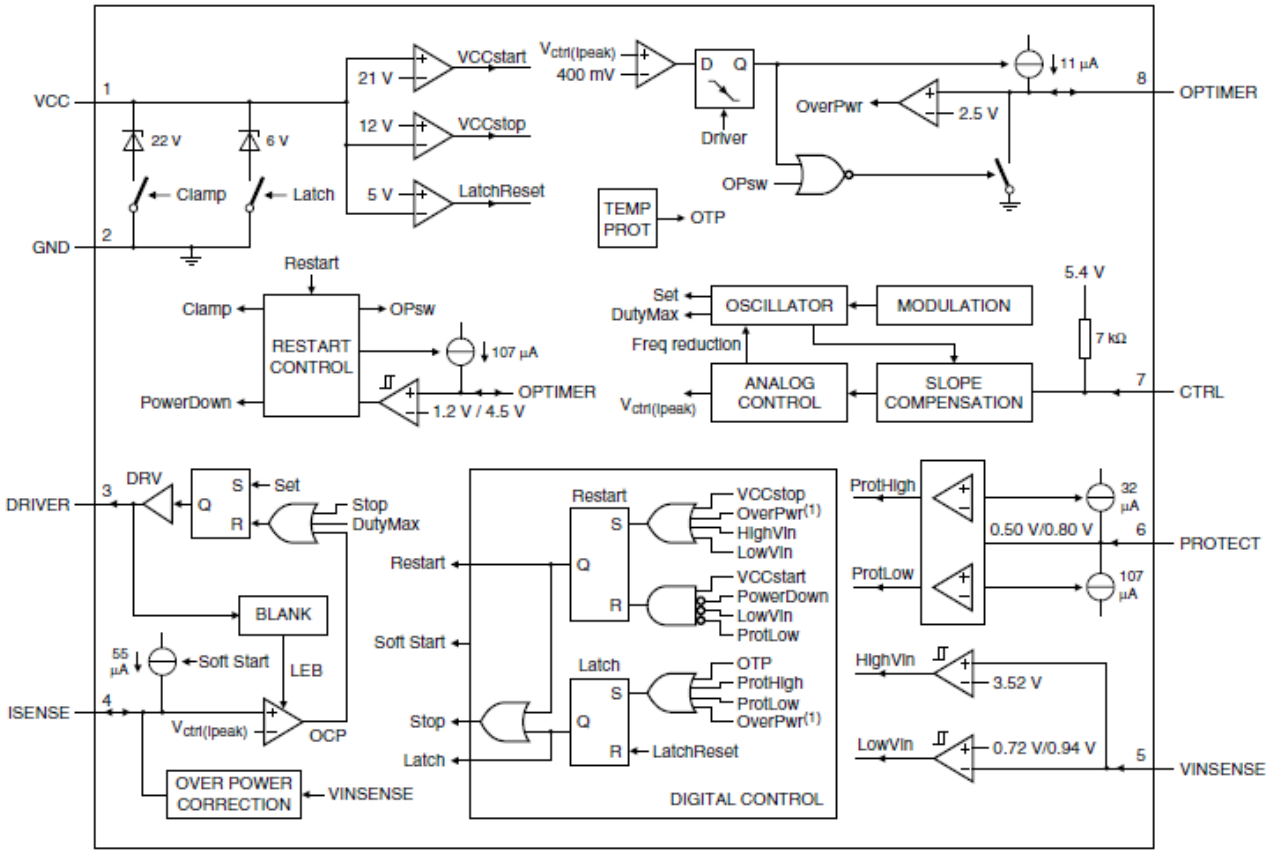
3.1.1 The main chip general description

The main chip of power supply is the TEA1733P which is produced by NXP corporation. The operating mode is CCM (continuous conduction mode), and the operating frequency is 65KHz.

3.1.2 The chip pin information



3.1.3 The chip block diagram



3.1.4 The IC pin description

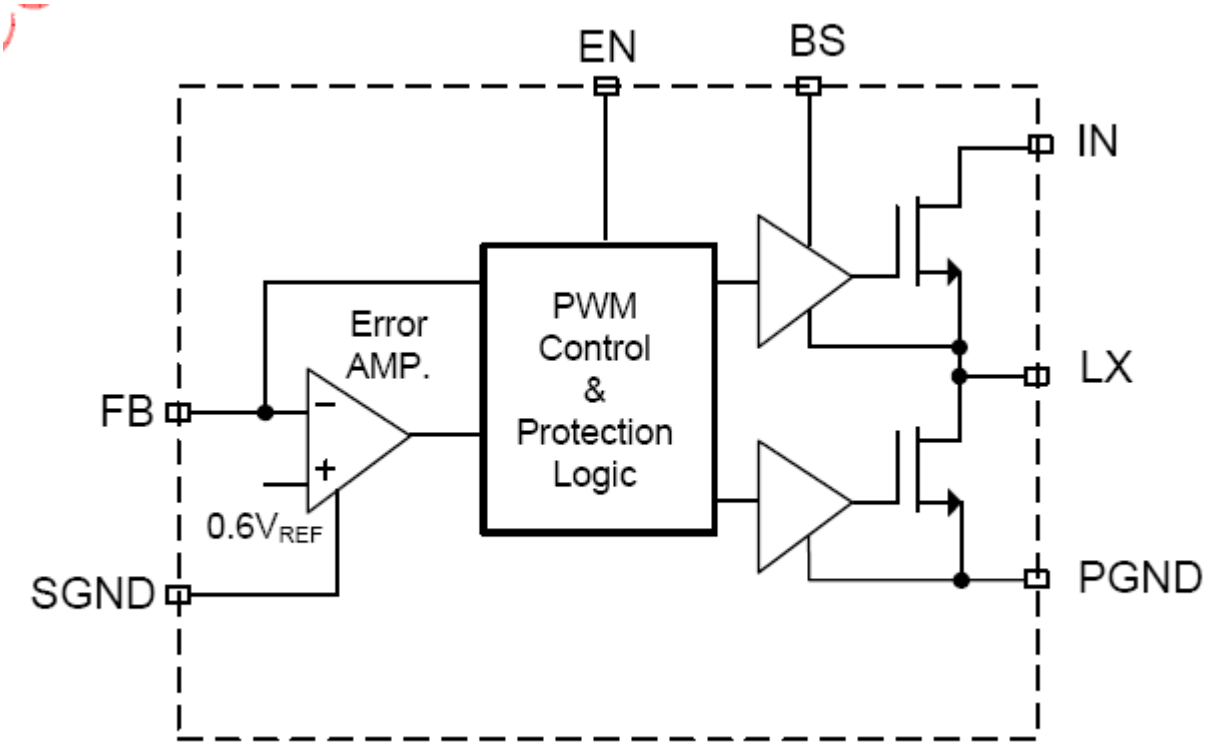
Symbol	Pin	Description
VCC	1	supply voltage
GND	2	ground
DRIVER	3	gate driver output
ISENSE	4	current sense input
VINSENSE	5	input voltage protection input
PROTECT	6	general purpose protection input
CTRL	7	control input
OPTIMER	8	overpower and restart timer

3.2 The DC-DC chip

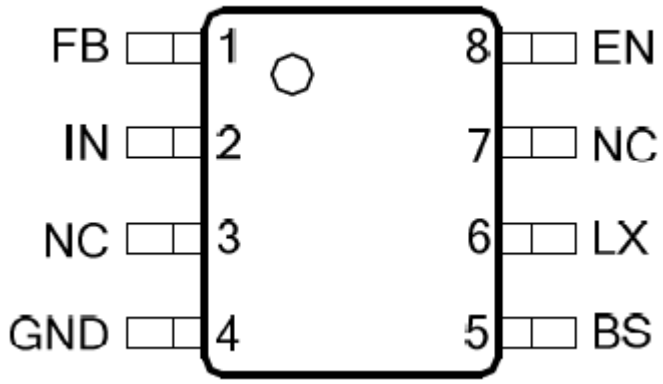
3.2.1 General description

The DC-DC used for standby chip, using SY8172Y, double synchronous rectification,and operating frequency is 700KHz.

3.2.2 The chip block diagram



3.2.3 The chip pin information



3.2.4 The pin description and the voltage

Pin Name	Pin Number	Pin Description
BS	5	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.
IN	2	Input pin. Decouple this pin to GND pin with at least 1uF ceramic cap
LX	6	Inductor pin. Connect this pin to the switching node of inductor
GND	4	Ground pin
FB	1	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R1/R2)
EN	8	Enable control. Pull high to turn on. Do not float.
NC	3,7	No connection.

(V_{IN} = 12V, V_{OUT} = 2.5V, L = 2.2uH, C_{OUT} = 10uF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

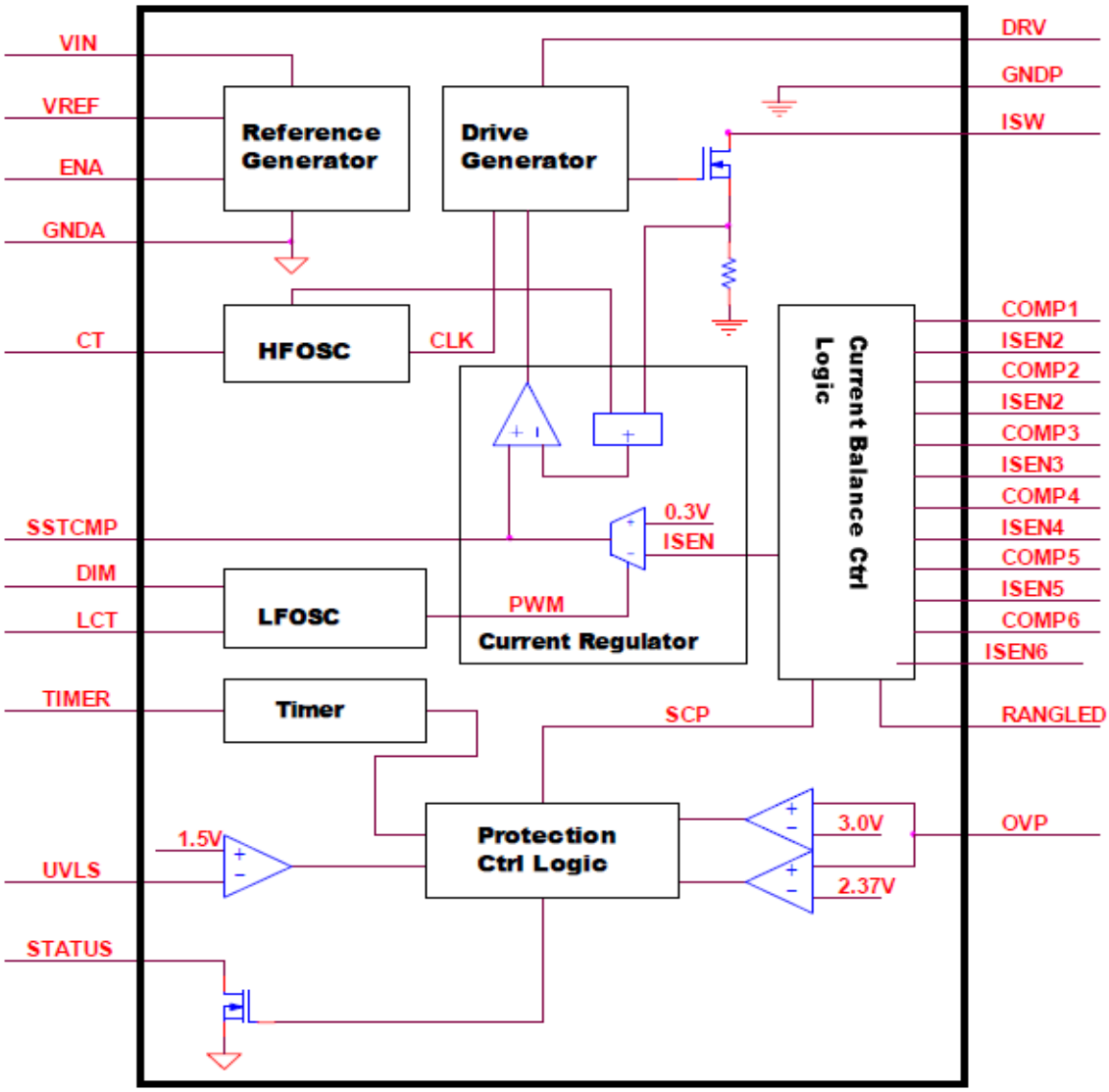
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		15	V
Quiescent Current	I_Q	$I_{OUT=0}$, $V_{FB}=V_{REF}\times105\%$		200		μA
Shutdown Current	I_{SHDN}	EN=0		1	5	μA
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
FB Input Current	I_{FB}	$V_{FB}=V_{IN}$	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			150		mΩ
Bottom FET RON	$R_{DS(ON)2}$			100		mΩ
Top FET Current Limit	I_{LIM}		2.4			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				3.9	V
UVLO Hysteresis	V_{HYS}			0.3		V
Oscillator Frequency	F_{OSC}	I_{OUT}=200mA		700		kHz
Min ON Time				50		ns
Max Duty Cycle			90			%
Thermal Shutdown Temperature	T_{SD}			160		°C

3.3 The LED driver chip

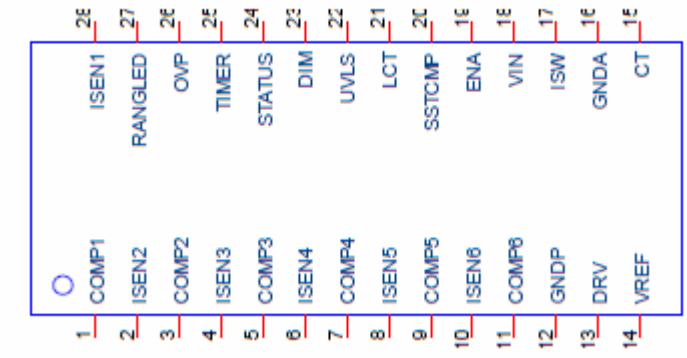
3.3.1 General description

The OZ9967 is an LED controller that drives a number of LEDs connected in serial or parallel configuration.

3.3.2 The chip block diagram



3.3.3 The chip pin information

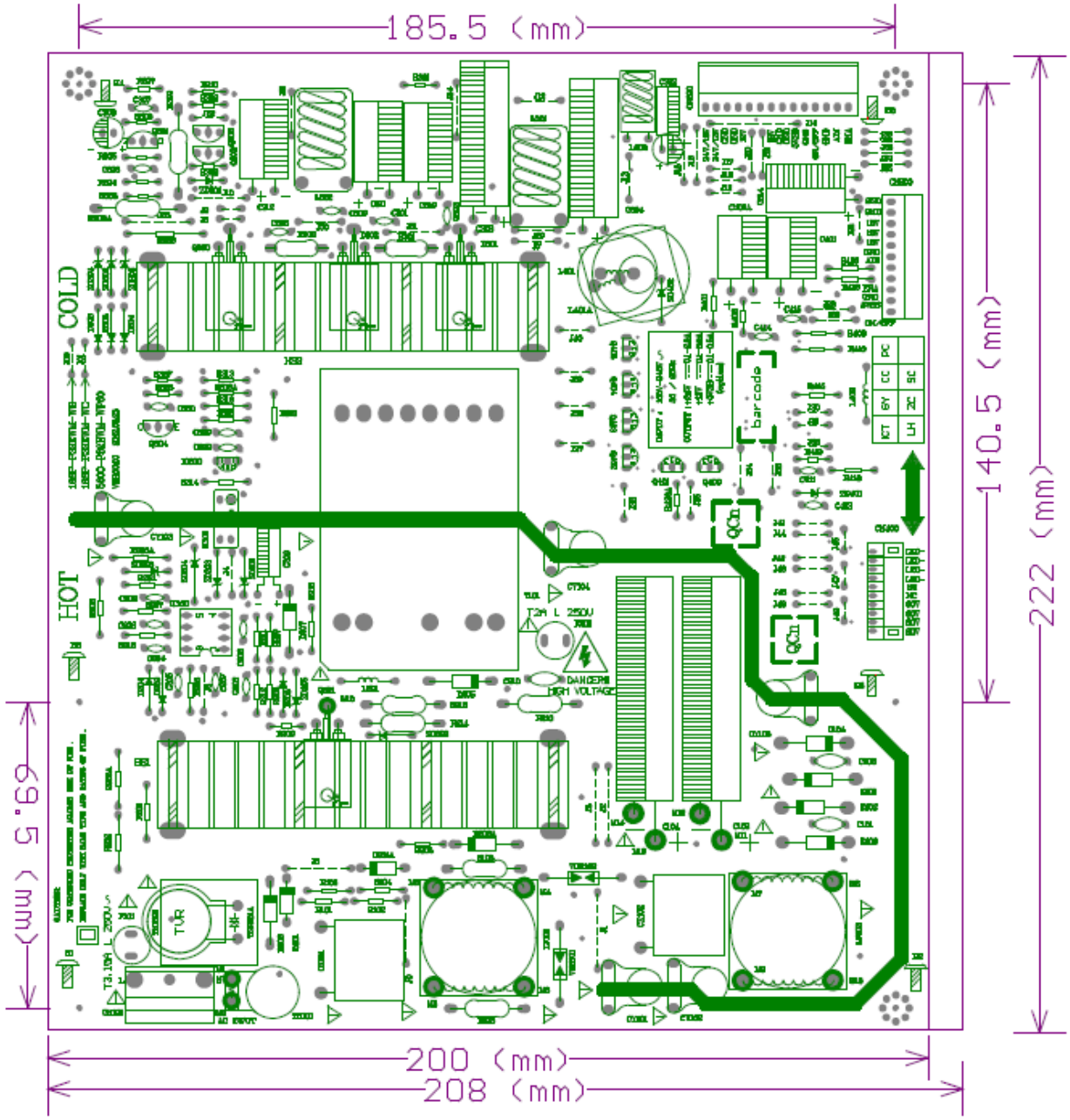


3.3.4 The **pin description and the voltage**

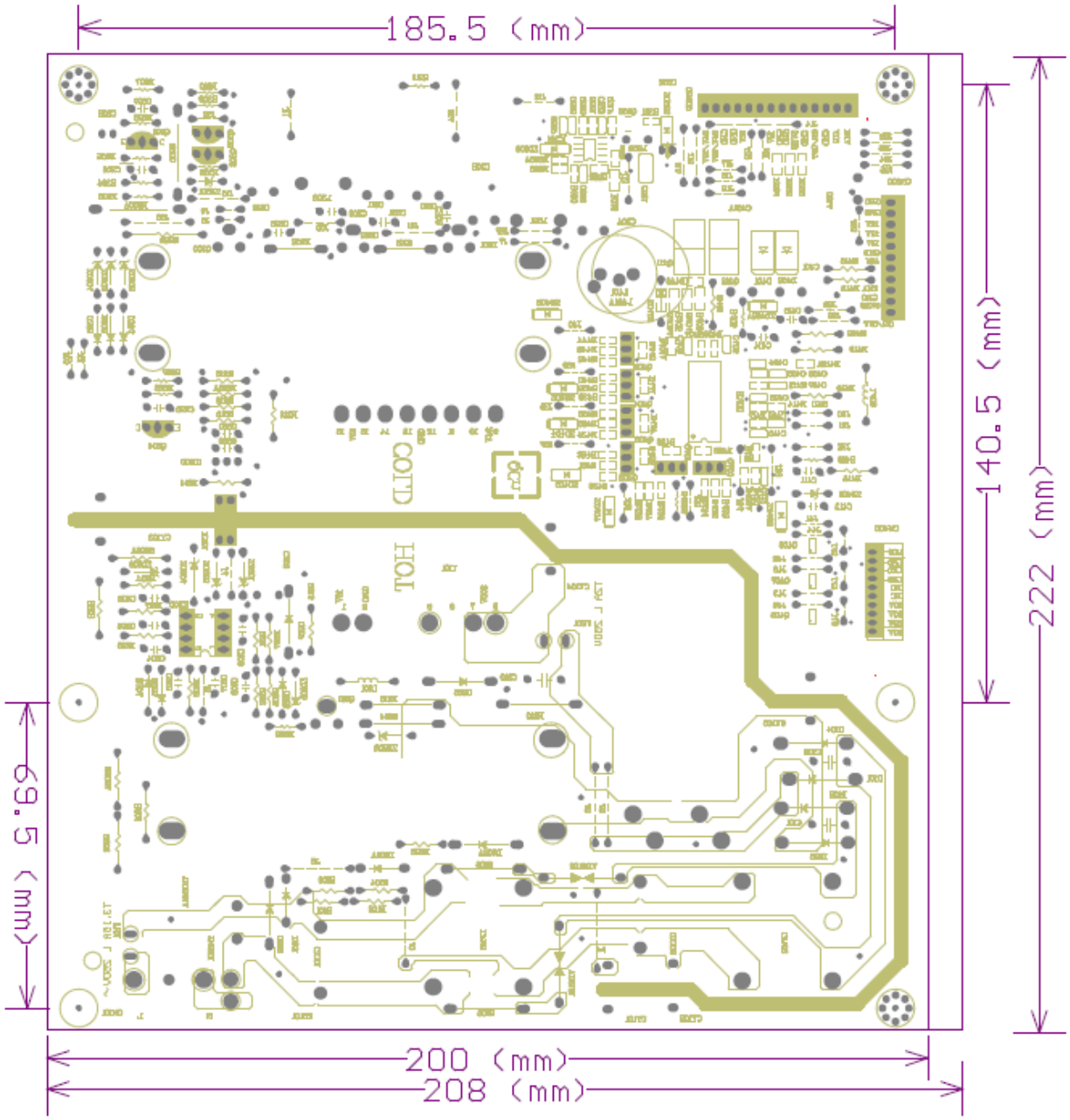
Pin No	I/O[1]	Name	Description
1	I/O	COMP1	Control signal for LED balance switch 1
2	I	ISEN2	LED current sense signal 2
3	I/O	COMP2	Control signal for LED balance switch 2
4	I	ISEN3	LED current sense signal 3
5	I/O	COMP3	Control signal for LED balance switch 3
6	I	ISEN4	LED current sense signal 4
7	I/O	COMP4	Control signal for LED balance switch 4
8	I	ISEN5	LED current sense signal 5
9	I/O	COMP5	Control signal for LED balance switch 5
10	I	ISEN6	LED current sense signal 6
11	I/O	COMP6	Control signal for LED balance switch 6
12	---	GNDP	Power ground
13	O	DRV	Power MOSFET drive signal
14	I/O	VREF	Reference voltage
15	I/O	CT	Timing resistor and capacitor for high frequency oscillator
16	---	GNDA	Signal ground
17	I/O	ISW	Power MOSFET current sense signal
18	---	VIN	Input voltage
19	I	ENA	Enable signal
20	I/O	SSTCMP	Soft-start and compensation
21	I/O	LCT	Timing resistor and capacitor for low frequency oscillator
22	I	UVLS	Input voltage under-voltage protection
23	I	DIM	Dimming control signal
24	O	STATUS	Controller status indicator
25	I/O	TIMER	Timing capacitor for delay timer
26	I/O	OVP	Over voltage protection sense signal
27	I	RANGLED	LED short protection threshold
28	I	ISEN1	LED current sense signal 1

4. PCB TopOverlay and BottomOverlay

4. 1 The power supply TopOverlay



4. 2 The power supply BottomOverlay



5. Maintenance instructions

5. 1 Common Fault Analysis and Notes

1. No +5VSB output voltage

If there is no +5VSB output voltage , we should focus on checking the DC-DC IC(IC301) and judge whether the IC is operating . Monitor its VIN pin and check voltage is normal or abnormal . If it is normal , firstly , check the DC-DC IC peripheral circuit . Secondly, check DC-DC IC(IC301)and judge it has broken or not. If the VIN pin voltage is abnormal, you need to check the IC100 power circuits.

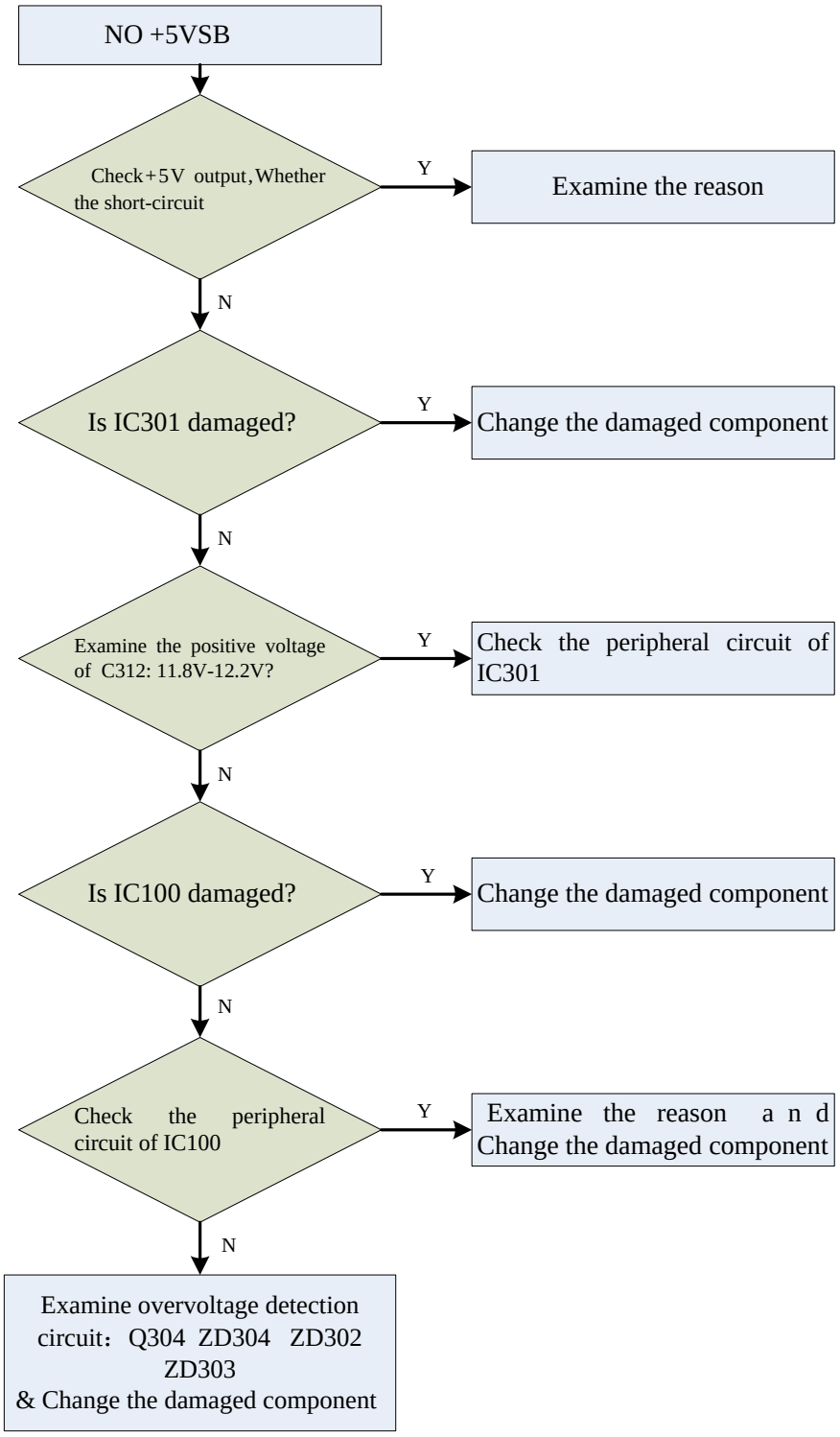
2.+5VSB output is normal ,+12V output is abnormal

First, check +12 V voltage of the MOS transistor(Q300) S pole is normal or abnormal , if it is normal,please check the MOS transistor(Q300) peripheral circuit is normal or not. If the +12 V voltage of the MOS transistor(Q300) S pole is abnormal, please check the IC100 circuits.

3.+5VSB is abnormal

Check the +5 VSB feedback loop , and the reference voltage of the IC301 is normal or not.

5.2 Service process



5.2 Port and the connection defined

5.2.1 PIN10 CN400 Connection And Function

NO.	Pin Connection	Function
1	LED-	LED-
2	LED-	LED-
3	LED-	LED-
4	LED-	LED-
5	NC	NC
6	NC	NC
7	60V	LED+
8	60V	LED+
9	60V	LED+
10	60V	LED+

Note: CN400 TYPE : 2.0mm

5.2.2 PIN14 CN300 Connection And Function

NO.	Pin Connection	Function
1	+24V	+24V DC OUTPUT
2	+24V	+24V DC OUTPUT
3	GND	GND
4	GND	GND
5	+12V	+12V DC OUTPUT
6	+12V	+12V DC OUTPUT
7	GND	GND
8	GND	GND
9	+5VSB	+5VSB DC OUTPUT
10	GND	GND
11	ON/OFF	POWER_ON/OFF
12	GND	GND
13	ADJ	BL_ADJUST
14	ENA	BL_ON/OFF

Note: CN300 TYPE : 2.5mm

5.3 Key components and service parts list

NO.	Material number	Material models	Position number	Function	Substitute Material	Remark
1	4706-B17330-0080	TEA1733P	IC100	Main chip		
2	47EC-S81721-0080	SY8172Y	IC301	DC-DC chip		
3	476K-Z99671-0280	OZ9967GN	IC400	LED driver chip		
4	4655-P27610-00	AOTF10N65	Q201	Main MOS		
5	4666-M15N10-0S00	ME15N10-G/TO252	Q412	Boost MOS		
6	451F-210200-0000	HBR10200HF	D301 D302	Secondary Schottky		
7	5132-064955-0000	SANHE-42-102	T101	transformer		
8	47AH-P817C0-04	BPC-817C0	IC101	Optocoupler		

5.4 Storage, transportation and using conditions

5.4.1 Package

Box must have the product name, model, identification，quality inspection department certification，the date of manufacture and so on.

5.4.2 Transportation

The productor adapted to cars, boats, aircraft transport .Transportation should be covered, prevented sunshine and loading lightly.

5.4.3 Storage

Products should be stored in a box if it is not used .The storehouse environment temperature is from -40 ℃ to -55 ℃, relatived humidity is from 10% to -95%. The storehouse must not allow any harmful gases, flammable ,explosive and corrosive product chemicals, and must not allow strong mechanical vibration, shock and strong magnetic field. Boxes should be at least 20cm high from the ground .The distance from the wall, heat source, windows or air enter is at least 50cm. The storage period is about two years, more than two years should be re-tested under the regulation .

6.Information of Power supply designers

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7. Schematic diagram